The SUPERNET®2 Family for FDDI
1991/1992 World Network™
Data Book

ADVANCED MICRO DEVICES

TABLE OF CONTENTS

Introduction 1–1

Am79C830A
FORMAC Plus 2–1

Am79C830
FORMAC Plus 2–3

Am79C864
Physical Layer Controller 3–1

Am79865/Am79866
Physical Data Transmitter/Physical Data Receiver 4–1

FASTcard 2 5–1

Physical Dimensions 6–1

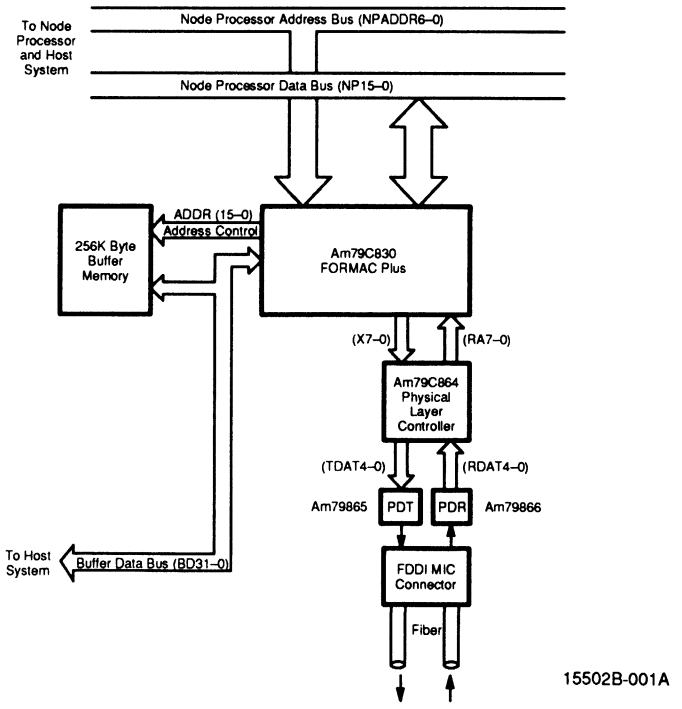
Appendix
Interface Connection Diagrams A–1

The SUPERNET®2 Family for FDDI
(Am79C830, Am79C864, Am79865, Am79866)

DISTINCTIVE CHARACTERISTICS

- Compliant with the ANSI X3T9.5/ISO 9314 specifications
  - 100 Mbps data rate
  - Timed token-passing protocol
  - Ring topology
- Complete memory management
  - Supports 256K bytes of local frame buffer memory
  - Supports buffer memory bandwidths of 200 Mbps to 400 Mbps
  - Non-Tag Mode: linked list transmit frame structure compatible with SUPERNET 1
  - Tag-Mode: minimum latency/highest performance buffer memory management, ideal for adapter card designs
- Full duplex operation: 200 Mbps continuous data rate
- Supports both fiber optic and copper media
- Diagnostic features
  - Multiple loopback modes for run-time diagnostics
  - Built In Self Test (BIST) in Physical Layer Controller (PLC)
- Hardware Physical Connection Management support
- Low power consumption—reduction of more than 50% from SUPERNET 1 solution

BLOCK DIAGRAM



SUPERNET 2 Chip-Set Interconnect Block Diagram for Single Attachment Station (SAS)

GENERAL DESCRIPTION

The ANSI X3T9.5/ISO 9314 specifications, named the Fiber Distributed Data Interface (FDDI), define a means of interconnecting equipment with a very high-speed network. Running at a data rate of 100 Mbps over fiber optic or copper twisted pair cable, this standard offers ten times the speed of Ethernet, excellent noise immunity, and a timed-token passing protocol which guarantees each node access to the network. The 4-chip SUPERNET 2 family implements the FDDI standards and offers a variety of additional system features.

SUPERNET 2 is a second generation FDDI chip-set from AMD. Like the first generation SUPERNET solution, SUPERNET 2 provides complete buffer management functions common to most network protocols. When used in non-tag mode, the FORMAC Plus replaces and is fully downward compatible with the previous generation three chip combination made up of the Am79C81A (RBC), the Am79C82A (DPC) and the Am79C83 (FORMAC). In tag-mode, the FORMAC Plus manages the buffer memory as multiple FIFOs.

There are two key advantages to tag-mode operation; 1) programmable transmit and receive thresholds allow early notification (receive) and transmission yielding absolute minimum frame latencies and 2) the multiple FIFO structure simplifies interfacing with the FORMAC Plus thus reducing software/hardware overhead. Because of these characteristics, tag-mode is particularly well suited to adapter cards and motherboards where the local memory is tuned to allow high performance operation with network and buffer latencies taken into consideration. For a more detailed understanding of buffer memory sizing in FDDI adapter designs, refer to AMD PID#16294A, "Sizing Local Buffer Memory in FDDI."

In addition to providing a software compatible upgrade path from SUPERNET 1, the linked-list data structure of non-tag mode is well suited for concentrator designs where the FORMAC Plus buffer memory is the target memory. In this case, frames can be operated on in the FORMAC Plus controlled buffer memory obviating the need for an additional component to perform "system interface functions."

The FORMAC Plus provides DMA channels, arbitrates access to the network buffer memory, and controls the data path between the buffer memory and the medium. The FORMAC Plus also fully implements the timed-token protocol and receive/transmit control specified for the Media Access Control (MAC) sublayer of the ISO standard 9314-2 for FDDI. Physical sublayer (PHY) tasks defined by the ISO standard 9314-1 are performed by a three-chip combination of the Am79C864 Physical Layer Controller (PLC), the Am79865 Physical Data Transmitter (PDT) and the Am79866 Physical Data Receiver (PDR). The three chips are collectively known as the AmPHY. The PDT/PDR connect to the fiber optic transceiver which converts an optical signal coming from the medium to an equivalent electrical logic signal or vice versa. The PDT/R devices can also drive copper media directly as shown in AMD PID#15923A/0, "FDDI on Copper with AMD PHY Components."

INTRODUCTION

The block diagram on page 1 shows AMD's SUPERNET 2 architecture which meets the ISO 9314 FDDI data communications standard. The primary function of the SUPERNET 2 chip-set is to act as an interface between a host computer and the network medium, using the FDDI protocol, to transfer and convert data between parallel form, at the host, and serial form, at the media.

SYSTEM DATA PATHS

The station receives data in serial form from the network medium. The fiber optic or copper transceiver interfaces the medium to the PDR. Using its clock recovery PLL, the PDR derives clocking information from the encoded stream and converts the bit stream to unframed 5-bit symbols. The PLC chip receives the symbol-wide (5-bit) data along with a 25 MHz recovered clock from the PDR and searches for a JK symbol pair, also known as the starting delimiter. The PLC uses a starting delimiter to establish byte boundaries and to frame the incoming data. The data is decoded and sent to the FORMAC Plus. The receive demultiplexer in the FORMAC Plus formats four bytes of data into a 32-bit long word which is temporarily stored in the receive FIFO until the buffer memory is ready to receive it. The FORMAC Plus sets up addresses on the 16-bit address bus to store the frame in buffer memory.

The data can then be sent to the host memory from the buffer memory on the 32-bit data bus. Initialization and control of the SUPERNET 2 chipset is realized through a node processor (NP) interface via a 16-bit bus called the NP bus. In addition, the NP interface provides an alternate access method to buffer memory using the MAR and MDR registers.

SYSTEMS COMPONENTS

Host Systems

The term "host" is used here to refer to any mainframe, workstation, minicomputer, or computer peripheral (such as a disk drive or a printer) to which a network interface is attached. In a large system, a powerful NP may be used to off-load various networking specific chores. In simpler systems, the host and NP may be one and the same, meaning that the host computer performs all NP functions. Lower-cost systems may use this configuration.

Node Processor

The Node Processor (NP) can be a microprogrammed or conventional microprocessor-based system used for overseeing the operation of the SUPERNET 2 chip-set. Its main function is to initialize the devices and respond to various system-level and frame-level interrupts. In the simplest case it can be a minimal state machine. More complex architectures can have all the sophistication required to execute the upper-layer protocols specified by the seven-layer International Standards Organization (ISO) Open System Interface (OSI) model.

The NP communicates with the SUPERNET 2 chip-set using the NP-bus and various bus handshakes and instructions lines. Its handshake with the Host system is user-defined and depends on the partitioning of functions between the Host and the Node Processor.

The NP can communicate with the buffer memory by issuing an NP memory request to the FORMAC Plus and, when access is granted, using the 32-bit data bus. An alternate method is provided through use of software instructions to the FORMAC Plus in conjunction with accessing the internal MAR and MDR registers. The 32-bit wide Memory Data Register (MDR) is used for data transfer between the node processor and buffer memory. A typical NP could consist of a microprocessor with assorted peripheral chips (for DMA, interrupts, etc.) and local memory. The NP treats the SUPERNET 2 chip-set as a peripheral for networking functions. The NP has complete control over (and knowledge of) the state of the SUPERNET 2 chip-set and buffer memory. These chips make their status available to the NP to help it maintain this control.

The NP can run either synchronously or asynchronously with respect to the network clock. Any required synchronization with tCs surrounding the SUPERNET chip-set is performed by the FORMAC Plus.

Buffer Memory

The Buffer memory, consisting of static RAM, is used for intermediate storage of frames. Its addresses are generated and controlled by the FORMAC Plus. The buffer memory cycles are controlled by a buffer memory clock (BMCLK) which is independent of the network clock. The BMCLK may have a frequency between 12.5 MHz and 25 MHz giving a total memory bandwidth of 200 Mbps to 400 Mbps. This allows for the possibility of operating on the frames as they reside in the buffer memory while leaving ample bandwidth to continue the exchange of frames on the network. Optionally, a node processor (NP) can do any processing necessary to assure the host that the frame is good. Finally, the frame is transferred to the host. Frame transmission is just the reverse. At a 100 Mbps data rate, a 70-ns access time is generally adequate. Both separate I/O and multiplexed I/O configurations can be used. As an option, the memory can be set up to be protected with byte parity.

The memory can be accessed by the FORMAC Plus, NP and the host. Only one of these can access the memory at any time, and the FORMAC Plus arbitrates all requests to determine who can access the memory.

Am79C830 Fiber Optic Media Access Controller (FORMAC) Plus

The FORMAC Plus performs the Media Access Control (MAC) layer protocol for the FDDI standard networking scheme. The FORMAC Plus determines when a node can get access to the network and implements the logic required for token handling, address recognition, and CRC.

Upon receiving a frame, the FORMAC Plus strips away all the physical layer headers. Any preamble or start of frame delimiters are detected and discarded. Also, any end-of-frame characters or postamble is removed. The FORMAC Plus checks incoming frames for destination address and when a match does occur the data from the received frame is loaded into the receive FIFO and the long words are transferred into buffer memory. It also generates and checks CRC on frames.

The FORMAC Plus's interface with the PLC consists of three 10-bit (eight data bits and two control bits) buses. Two of these handle received data frames, while the third is used for data transmission. Data on these buses move synchronously with the byte rate clock (BCLK).

Am79C864 Physical Layer Controller (PLC)

The PLC, along with the PDT and PDR, perform the Physical sub-layer (PHY) protocol and portions of Station Management (SMT) for the FDDI standard.

The FORMAC Plus transmits data frames in the form of 8-bit bytes accompanied by two control characters. The PLC receives byte-wide data from the MAC at 12.5 million bytes per second, then performs 4B/5B encoding which maintains the DC balance in the output waveform and guarantees that no more than three consecutive 0's will be present in an encoded pattern. The encoded data is sent out symbol-wide at 25 million symbols per second to the PDT. The repeat filter in the transmit path detects corrupted symbols and converts them into a specific pattern of HALT and Idle symbols.

During frame reception, the PLC receives symbol-wide (5 bits) data along with a 25 MHz clock. The PLC frames data using the start delimiter. The framed data is then sent to the Elasticity Buffer which serves to compensate for the frequency difference between the recovered clock and the local clock. The data is then decoded and sent to the FORMAC Plus. The data is byte-wide (10bits) and clocked by a 12.5 MHz local clock.

The PLC also communicates with the NP to force FDDI-specified line states onto the medium and performs various loopback functions and BIST.

Some functions specific to Station Management is also performed by the PLC. The PLC chip contains the Physical Connection Management (PCM) state machine which determines the timing and state requirement. Also contained in the PLC is the Physical Connection Insertion (PCI) state machine which performs the necessary ring scrubbing and data path switching.

Am79865 Physical Data Transmitter (PDT)/Am79866 Physical Data Receiver (PDR)

The PDT in the transmit path converts the symbol-wide data received from the PLC to serial format and sends an NRZI (non-return-to-zero, inverted on ones) bit stream to the fiber optic transmitter. The on-chip PLL in the PDT, driven by a 25 MHz external crystal controlled clock source, generates a bit rate clock.

The PDR receives serial NRZI data stream and converts them to NRZ. Using its on-chip PLL, the PDR extracts encoded clock information from the serial NRZI data stream and recovers the data. The recovered clock is used for the serial-to-parallel data conversion. The PDR provides a symbol-wide unframed data to the PLC.

Fiber Optic Transceiver

Fiber optic receivers typically consists of a pin diode, amplifier, equalizer, automatic gain control circuit, and comparator. The PIN diode receives an optical signal from the fiber and converts it into an electrical waveform. The signal is then amplified and conditioned. Amplifier gain is variable and depends on the magnitude of the incoming signal. The conditioned waveform is then passed through comparator which determined whether the output should be a logic "1" or "0". The resulting bit stream is then fed to the PDR with a pair of differential drivers.

The fiber optic transmitter accepts a differential signal from the PDT and, by means of a light-emitting diode (LED), converts it into an optical output for transmission onto the fiber optic cable.

SYSTEM BANDWIDTH

The SUPERNET 2 chip-set is designed to provide the maximum data rate of 100 Mbps on the network medium. This speed implies that the buffer memory bus on the FORMAC Plus can support a minimum data rate of 12.5 MBytes/sec, the equivalent of 100 Mbps. Figure 1 shows the bandwidth provided in the complete system. The buffer memory interface is designed to support 200-Mbps to 400-Mbps sustained transfer rates on the 32-bit buffer memory bus. This translates to a minimum rate of 25 MBytes/sec or 6.25 Mega "long words"/sec at the buffer memory. Therefore, at 12.5 MHz with network transmit or receive occurring (100 Mbps) at a node, only half the memory bandwidth is used by the FORMAC Plus for reception or transmission of frames. The remaining 100 Mbps bandwidth on the memory is available to either the NP or the host. At 25 MHz, only one fourth of the bandwidth is required for network activity leaving 300Mbps of bandwidth available. The FORMAC Plus lets the NP or the host share this bandwidth through cycle stealing while frames are transferred. When the FORMAC Plus is neither transmitting nor receiving, the complete bandwidth of the buffer memory can be available to the NP or the Host. This bandwidth may be used by either the NP or host exclusively, or shared between the two.

This ample availability of memory bandwidth is provided to minimize the buffer space required. SUPERNET 2 allows partial or complete frames to be emptied as they are received. Buffers can be small and the node interface can be simple.

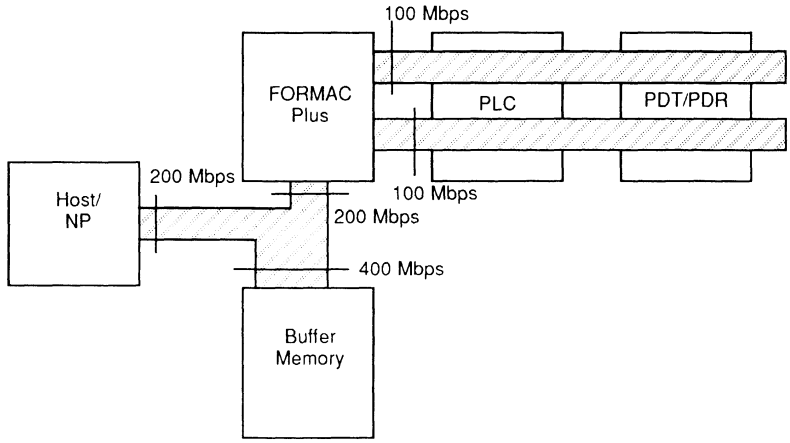


Figure 1. System Bandwidth

ADVANCE INFORMATION

Am79C830A

Formac Plus

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Am79C830 with enhanced features**
- **Supports Void Frame Stripping in on-line special mode**

  When programmed to operate in the "on-line special" mode, the FORMAC Plus will issue two auto void frames prior to releasing the token. With the internal counter, the void and counter stripping algorithm can be implemented as described in both the bridge networking group documents of ANSI X3T9.5 and the IEEE 802.1D standard.
- **MAC Status Copying (MSC) Handling of A & C indicators**

  When the FORMAC Plus is programmed to operate in the "on-line special" mode, the A & C indicators will be set in accordance with the bridge type described as "MAC Status Copying" (MSC) when the external destination address match signal (XDAMAT) is activated. The A & C indicators will be handled normally for addresses recognized through the internal FORMAC Plus registers.
- **SRCOMP bit functional in Tag Mode**

  The SRCOMP bit in status register two upper will be valid in tag mode. The SRCOMP bit indicates that the status word has been written to the buffer memory following the reception of a frame. In Am79C830, this bit is meaningful only in non-tag mode. The SRCOMP bit will now also indicate when the status word is written into the buffer memory in tag mode as well as non-tag mode.
- **Timer for detection of duplicate MAC addresses**

  When the ring is not operational, during claim or beacon states, the TSYNC timer is utilized to time transitions RM34a and RM34b of the Ring Management (RMT) state machine. The timer is initialized with a value of twice Dmax (3.546 ms). It begins to count as the MAC transmit state machine takes transitions T45 (claim state to beacon state) or T54 (beacon state to claim state). It is reinitialized at the transition between claim and beacon states. If the timer expires while the MAC is still in T4 or T5 and MY_CLAIM or MY_BEACON is received, the existence of a duplicate MAC address on the ring is detected. This will be indicated by setting SDUPCLM (bit 2) in status register 2 lower.

GENERAL DESCRIPTION

The Am79C830A is an enhanced version of the current Am79C830. The enhancement incorporates new functions to support transparent bridging in addition to other new features. This an identical device to Am79C830 with respect to pin-outs and dimensions. Contact your local AMD sales office for more information.

Publication# 16287 Rev. A Amendment/0
Issue Date: September 1991

PRELIMINARY

Am79C830

FORMAC Plus

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Implements the FDDI Media Access Control (MAC) layer protocol for ISO standard 9314-2**
- **Buffer-memory clock frequency range:** 12.5 MHz to 25 MHz
- **Full-duplex operation: 200 Mbps continuous data rate**
- **Supports buffer memory bandwidths of 200 Mbps to 400 Mbps**
- **Full support for synchronous transmission**
- **Three asynchronous priority queues with individually programmable threshold levels**
- **Two basic modes of operation:**

  Nontag mode: On a per-frame basis, identical in operation with the AMD RBC/DPC/FORMAC combination

  Tag Mode: Operates on partial frames in buffer memory for both transmit and receive, allowing for reduced buffer-memory requirements and increased station data throughput
- **Pointers to claim and beacon frames**
- **Supports transmit linked-list addressing**
- **Integrated buffer-memory management:**

  DMA arbitration between NP, buffer memory, and host interfaces

  MAC of choice for FDDI concentrators. Handles SMT and MAC frames without the need for complex network DMA function
- **Bridging features:**

  Control of CRC on a per-frame basis

  Control of A and C bits

  External address-match support

  Programmable delay for frame flushing

  Tag mode allows maximized frame-forwarding rates

GENERAL DESCRIPTION

The Am79C830 FORMAC Plus implements the timed-token protocol and receive/transmit control specified for the Media Access Control (MAC) sublayer of the ISO Standard 9314-2 describing the Fiber Distributed Data Interface (FDDI). The FORMAC Plus is a CMOS device that provides in a single chip an interface between the physical layer of a station on an FDDI network, and the station's memory. Also provided on the Am79C830 is its interface to a host system and a complete interface to a buffer memory for transmitted and received data. The FORMAC Plus operates in either of two modes. In one mode (called the nontag mode), it replaces and is fully downward compatible with the previous-generation SUPERNET 1 three-chip combination made up of the Am79C81A (RBC), the Am79C82A (DPC), and the Am79C83 (FORMAC). In its second mode (called the tag mode), in addition to having the full operational capabilities of the nontag mode, FORMAC Plus transforms the associated buffer memory into multiple FIFOs, thus reducing data movement within the buffer memory and substantially improving throughput. Other FORMAC Plus features include on-chip receive and transmit FIFOs; separate receive and transmit CRC generation and checking logic; SMT capabilities; and three separately-prioritized asynchronous queues.

Publication# 14977 Rev. B Amendment/0
Issue Date: October 1991

BLOCK DIAGRAM

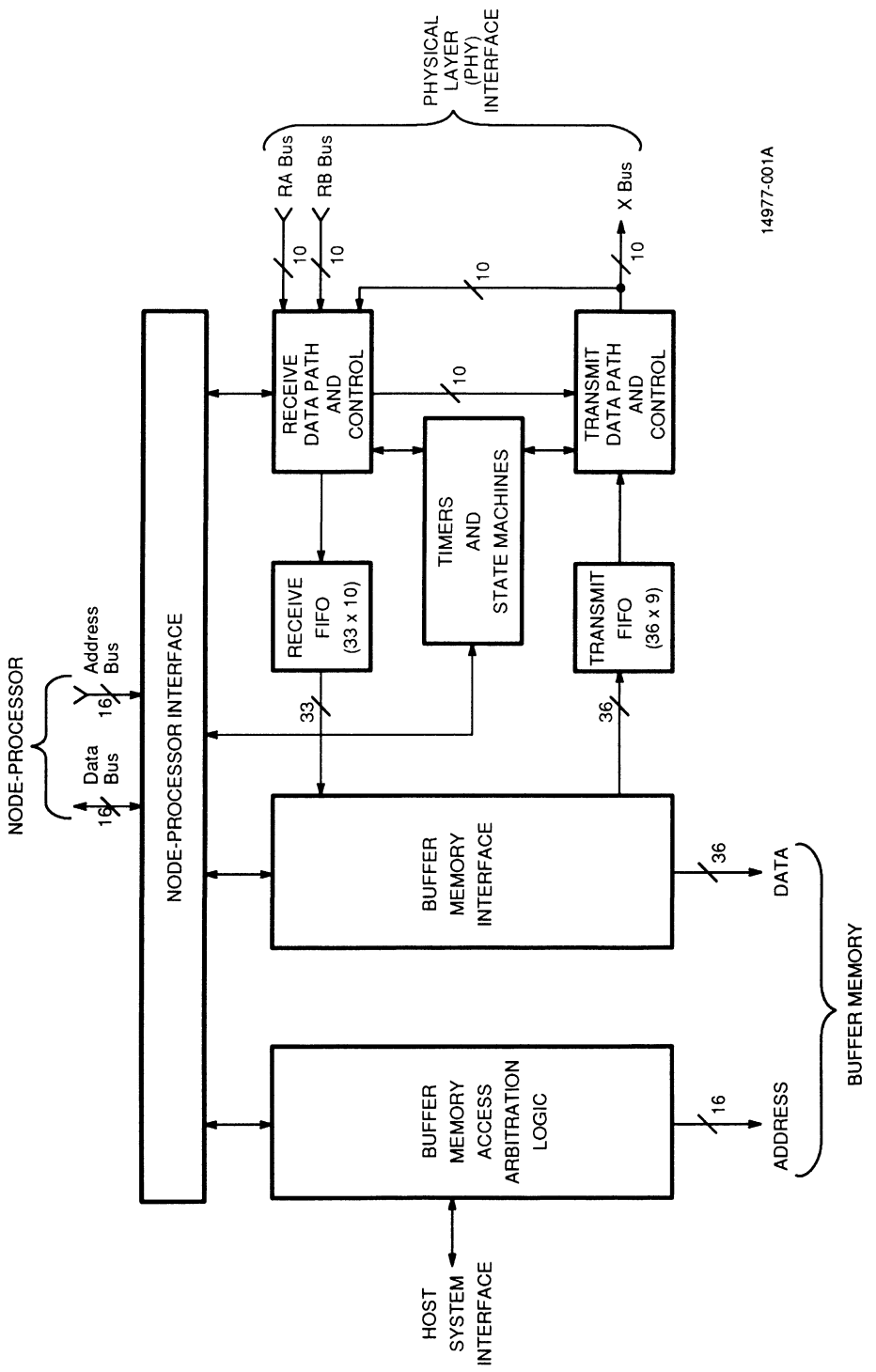


TABLE OF CONTENTS

DISTINCTIVE CHARACTERISTICS 2–3

GENERAL DESCRIPTION 2–3

BLOCK DIAGRAM 2–4

TABLE OF CONTENTS 2–5

169-Pin PGA CONNECTION DIAGRAM 2–11

169-Pin PGA PIN DESIGNATIONS 2–12

168-Pin PQFP CONNECTION DIAGRAM 2–16

168-Pin PQFP PIN DESIGNATIONS 2–17

LOGIC SYMBOL 2–21

ORDERING INFORMATION 2–22

PIN DESCRIPTION 2–23
- Physical Layer (PHY) Interface 2–23
- Node Processor (NP) Interface 2–23
- Buffer Memory Interface 2–25
- Host/Buffer Memory Interface 2–26
- Node Processor (NP)/Buffer Memory Interface 2–27
- Special Functions 2–28
- Other Signals 2–30
- Power and Ground 2–31

INTERFACE DESCRIPTION 2–32
- Physical Layer (PHY) Interface 2–32
- Node Processor (NP) Interface 2–32
- Buffer Memory Interface 2–32
- Host interface 2–32
- Node Processor to Buffer Memory Interface 2–32
- Special Interface Lines 2–32

FUNCTIONAL DESCRIPTION 2–33
- Receive Data Path 2–33
  - General 2–33
  - Input Multiplexer 2–33
  - Receive CRC Checker 2–33
  - Symbol Filter 2–33
- MAC Receive Control 2–35
  - General 2–35

Receive State Machine 2–35
  - Address Detection Logic 2–35
  - Frame Status Logic 2–35
- MAC Timers 2–35
  - General 2–35

Timer Logic ... 2–35
Synchronous and Asynchronous Queue Timing ... 2–35
Receive Demultiplexer ... 2–36
Receive FIFO Read/Write Control ... 2–36
Receive FIFO ... 2–36
Buffer-Memory Interface ... 2–36
Memory Data Register (MDR) ... 2–36
Node-Processor (NP) Interface ... 2–36
Command Decoder and Status Registers ... 2–36
Buffer Memory Address File ... 2–36
Buffer Memory Address Generator ... 2–37
Buffer Memory Queue Counters ... 2–37
Introduction ... 2–37
Almost-Full Detection ... 2–37
Threshold Detection ... 2–37
Buffer Memory Access Arbitration Logic ... 2–37
Buffer Memory Address Drivers ... 2–37
Transmit FIFO ... 2–37
Transmit FIFO Read/Write Control ... 2–37
Transmit Multiplexer ... 2–38
Transmit Data Path ... 2–38
General ... 2–38
Input to Transmit Data Path ... 2–38
Adding CRC to Transmitted Frames ... 2–38
Adding Control Symbols to Transmitted Frames ... 2–38
MAC Transmit Control ... 2–38

FORMAC Plus OPERATIONAL MODES ... 2–39
Introduction ... 2–39
(1) Initialization Mode ... 2–39
(2) Memory Active Mode ... 2–39
(3) On-line Mode ... 2–39
Receive State ... 2–39
Frame Reception ... 2–40
Frame Flushing ... 2–40
Frame Flushing in Tag Mode ... 2–40
Frame Flushing in Nontag Mode ... 2–40
Frame Flushing of Stripped and Lost Frames ... 2–41
Frame Abort ... 2–41
Frame Stripping (Non-Repeat to Ring) ... 2–41
Frame-Status (FS) Handling ... 2–41
Non-Repeated Frames ... 2–42
Special Functions ... 2–42
Transmit State ... 2–42
Introduction ... 2–42
Frame Transmission ... 2–43
Recovery Operation ... 2–44

(4) On-Line Special Mode 2–44
(5) Loopback Mode 2–44

NODE PROCESSOR BUS OPERATION 2–45
Synchronous Mode 2–45
Asynchronous Mode 2–45

BUFFER MEMORY OPERATION 2–48
Introduction 2–48
Tag Mode 2–49
Loading of Transmit Frames (Tag Mode) 2–49
Frame Transmission from Buffer Memory (Tag Mode) 2–51
Transmitting Send-Immediate Frames from Buffer Memory (Tag Mode) 2–51
Loading of Claim/Beacon/Auto-Void Frames (Tag Mode) 2–51
Transmitting Claim/Beacon/Auto-Void Frames (Tag Mode) 2–52
Loading Receive Frames into Buffer Memory (Tag Mode) 2–52
Unloading Receive Frames from Buffer Memory (Tag Mode) 2–54
Nontag Mode 2–54
Loading Transmit Frames (Nontag Mode) 2–54
Chained Transmit Operation (Nontag Mode) 2–54
Transmission of Transmit Frames (Nontag Mode) 2–56
Loading Claim/Beacon/Auto-Void Frames (Nontag Mode) 2–57
Transmitting Claim/beacon/Auto-Void Frames (Nontag Mode) 2–57
Send-Immediate Frames (Nontag Mode) 2–57
Loading Receive Frames (Nontag Mode) 2–57
Unloading Receive Frames (Nontag Mode) 2–59

INTERFACING WITH THE PHYSICAL LAYER 2–60

STATUS AND INTERRUPTS 2–60
Introduction 2–60
Status Register 1 (ST1) 2–60
Status Register 2 (ST2) 2–64

DATA HANDLING AND FORMATS 2–67
Data Format of Transmit Frames in Buffer Memory 2–67
Introduction 2–67
Transmit Descriptor Format 2–68
Transmit Pointer Format (Nontag Mode only) 2–69
Data Format of Receive Frames in Buffer Memory 2–69
Introduction 2–69
Format of Receive Status-Word 2–69

FDDI FRAME FORMAT 2–73

CONFIGURATION-STRAPPING of FORMAC-Plus PINS 2–74

PROGRAMMING THE FORMAC Plus 2–74
Table of Programmable Resources 2–74
Programming the Mode Registers 2–79
Mode Register 1 (MDREG1) 2–79

Mode Register 2 (MDREG2) ... 2–84
Command Registers 1 and 2 and their Instruction Set ... 2–86
Command Register 1 ... 2–87
Send-Immediate Commands ... 2–90
Command Register 2 ... 2–90
Initialization Values for Timers, Counters and Related Registers ... 2–91
FDDI Timer Implememtation ... 2–92
Station-Address Registers ... 2–92
MAC Information Register (MIR) ... 2–92
Priority Sequence Registers (PRI2-0) ... 2–92
Timer and Counter Registers ... 2–92
TMAX Register ... 2–92
TVX Register and Timer (Valid Transmission Timer) ... 2–93
Requested TRT Register (TREQ) ... 2–93
Token Rotation Timer (TRT) ... 2–93
Token Holding Timer (THT) ... 2–93
Negotiated TRT Register (TNEG) ... 2–93
Synchronous-Transmission Bandwidth Register and
TMSYNC Timer (TSYNC and TMSYNC) ... 2–93
Frame Counter (FCNTR) ... 2–94
Error Counter (ECNTR) ... 2–94
Lost Counter (LCNTR) ... 2–94
TMRS Register ... 2–94
MAC State-Machine Register ... 2–94
Programming the Buffer Memory Management Registers ... 2–95
Reset status ... 2–95
Buffer Memory Management Registers in Nontag Mode ... 2–95
Buffer Memory Management Registers in Tag Mode ... 2–96
Frame Threshold Register (FRMTHR) ... 2–97
Memory Address Register for Random Reads (MARR) ... 2–98
Memory Address Register for Random Writes (MARW) ... 2–98
Memory Data Register for Random Access (MDR) ... 2–98

SPECIFICATIONS ... 2–99
FORMAC Plus Functional Timings ... 2–99
Absolute Maximum Ratings ... 2–111
Operating Ranges ... 2–111
DC Characteristics Over Commercial Operating Ranges ... 2–111
Capacitance ... 2–111
Switching Characteristics Over Commercial Operating Ranges ... 2–112
Switching Waveforms ... 2–116
Switching Test Circuit ... 2–126
Switching Test Waveforms ... 2–127

APPENDIX A
GLOSSARY OF FORMAC Plus MNEMONICS ... 2–128

APPENDIX B
SUMMARY TABLES DESCRIBING FORMAC PLUS STATUS REGISTERS AND MODE REGISTERS ... 2–136

FIGURE LIST

BLOCK DIAGRAM 2–4

169-Pin PGA CONNECTION DIAGRAM 2–11

168-Pin PQFP CONNECTION DIAGRAM 2–16

LOGIC SYMBOL 2–21

ORDERING INFORMATION 2–22

1. FORMAC Plus FUNCTIONAL BLOCK DIAGRAM 2–34
2. NP Bus Synchronous Read/Write Cycles 2–45
3. NP Bus Synchronous MDRU/MDRL Read/Write Cycles 2–46
4. NP Bus Asynchronous Read/Write Cycles 2–47
5. Buffer Memory Organization (Tag and Nontag Modes) 2–49
6. Buffer Memory Transmit Queue (Tag Mode) 2–50
7. Buffer Memory Receive Queue (Tag Mode) 2–53
8. Buffer Memory Transmit Queue (Nontag Mode) 2–55
9. Buffer Memory Transmit Chain (Nontag Mode) 2–56
10. Buffer Memory Receive Queue (Nontag Mode) 2–58
11. Status Register 1: Upper 16 Bits (ST1U) 2–61
12. Status Register 1: Lower 16 Bits (ST1L) 2–61
13. Status Register 2: Upper 16 Bits (ST2U) 2–62
14. Status Register 2: Lower 16 Bits (ST2L) 2–62
15. Format of Transmit Descriptor (Tag and Nontag Mode) 2–67
16. Format of a Pointer (Nontag Mode) 2–67
17. Receive Frame Status Word 2–70
18. FDDI Frame Format 2–73
19. Mode Register 1 (MDREG1) 2–80
20. Mode Register 2 (MDREG2) 2–85
21. State Diagram for Interaction of Restricted and Nonrestricted Token Modes 2–89
22. MAC State Machine Register 2–95
23. Frame Threshold Register 2–97
24. Host and FORMAC Plus Buffer Memory Access Timing (Back-to-Back Read) 2–99
25. Host and FORMAC Plus Buffer Memory Access Timing (Back-to-Back Write) 2–100
26. NP (DMA) Buffer Memory Access: Normal Handshake 2–101

27. NP (DMA) Buffer Memory Access: Preemptive Host Write 2–102
28. NP (DMA) Buffer Memory Access: Preemptive FORMAC Plus Write 2–103
29. Host-Read Receive Queue 2–104
30. FORMAC Plus Buffer Memory Access 2–105
31. QCTRL and RDATA Operation During Host Buffer Memory Access 2–106
32. Transmit Signals Timing 2–107
33. Receive Status-Signals Timing 2–108
34. External Address Detection 2–109
35. Hold Operation 2–110
36. Node Processor (NP) Synchronous Read Timings 2–116
37. Node Processor (NP) Synchronous Write Timings 2–117
38. Node Processor (NP) Asynchronous Read Timings 2–118
39. Node Processor (NP) Asynchronous Write Timings 2–119
40. Physical Layer (PHY) Interface Timings 2–120
41 Host Interface Signal Timings 2–121
42. Buffer Memory Read Cycle Timings 2–122
43. Buffer Memory Write Cycle Timings 2–123
44. Node Processor (NP) DMA Cycle Timings 2–124
45. Miscellaneous Signals: AC Timings 2–125
46. Input Waveform Test Points 2–127
47. Output Waveform Test Points 2–127

CONNECTION DIAGRAM
169-Pin PGA Bottom View (Pins Facing Up)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	
1	HSREQ2	$\overline{RST}$	NPADDR4	NPADDR3	NPADDR0	NP14	NP12	NP10	BCLK	NP7	NP6	NP3	NP1	$\overline{DS}$ ($\overline{AS}$)	$\overline{MINTR1}$	$\overline{XDAMAT}$	RACL	1
2	RDATA	HSREQ0	NPMEMRQ	NPADDR6	NPADDR2	BMCLK	NP13	NP11	NP9	NP8	NP5	NP2	$\overline{CS1}$	R/$\overline{W}$	$\overline{MINTR2}$	$\overline{XSAMAT}$	RA5	2
3	QCTRL1	HSACK	HSREQ1	NPMODE	NPADDR5	NPADDR1	NP15	GND	VCC	GND	NP4	NP0	$\overline{READY}$	HOLD/XMTINH	RACU	RA7	RA4	3
4	ADDR15	QCTRL2	NPMEMACK	KEY ●											RA6	RA3	RA1	4
5	ADDR14	QCTRL0	GND												RA2	RA0	RBCL	5
6	ADDR12	ADDR13	GND												RBCU	RB7	RB6	6
7	ADDR10	ADDR11	VCC												GND	RB5	RB4	7
8	ADDR8	ADDR9	VCC												GND	RB3	RB2	8
9	ADDR7	ADDR6	VCC			**FORMAC Plus – Am79C830 169 PIN PGA**									GND	RB0	RB1	9
10	ADDR5	ADDR4	VCC												GND	RS3	RS4	10
11	ADDR3	ADDR2	VCC												VCC	RS1	RS2	11
12	ADDR1	ADDR0	GND												GND	XCU	RS0	12
13	$\overline{CS0}$	$\overline{WR}$	GND												X3	X6	XCL	13
14	$\overline{RD}$	BDTAG	GND												X0	X4	X7	14
15	BD0	BD1	BD3	GND	GND	GND	VCC	VCC	VCC	GND	GND	GND	BD30	BDP1	XS0	X1	X5	15
16	BD2	BD4	BD6	BD8	BD10	BD13	BD15	BD17	BD20	BD22	BD24	BD26	BD28	BD31	BDP2	XS1	X2	16
17	BD5	BD7	BD9	BD11	BD12	BD14	BD16	BD18	BD19	BD21	BD23	BD25	BD27	BD29	BDP0	BDP3	XS2	17
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	

14977-002A

PGA PIN DESIGNATIONS
(Listed by Pin Number)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
HSREQ2	A-1	NPADDR4	C-1	BD14	F-17	GND	M-15
RDATA	A-2	NPMEMRQ	C-2	NP12	G-1	BD26	M-16
QCTRL1	A-3	HSREQ1	C-3	NP13	G-2	BD25	M-17
ADDR15	A-4	NPMEMACK	C-4	NP15	G-3	NP1	N-1
ADDR14	A-5	GND	C-5	VCC	G-15	$\overline{CSI}$	N-2
ADDR12	A-6	GND	C-6	BD15	G-16	$\overline{READY}$	N-3
ADDR10	A-7	VCC	C-7	BD16	G-17	BD30	N-15
ADDR8	A-8	VCC	C-8	NP10	H-1	BD28	N-16
ADDR7	A-9	VCC	C-9	NP11	H-2	BD27	N-17
ADDR5	A-10	VCC	C-10	GND	H-3	$\overline{DS}$ ($\overline{AS}$)	P-1
ADDR3	A-11	VCC	C-11	VCC	H-15	R/$\overline{W}$	P-2
ADDR1	A-12	GND	C-12	BD17	H-16	HOLD/XMTINH	P-3
$\overline{CSO}$	A-13	GND	C-13	BD18	H-17	BDP1	P-15
$\overline{RD}$	A-14	GND	C-14	BCLK	J-1	BD31	P-16
BD0	A-15	BD3	C-15	NP9	J-2	BD29	P-17
BD2	A-16	BD6	C-16	VCC	J-3	$\overline{MINTR1}$	R-1
BD5	A-17	BD9	C-17	VCC	J-15	$\overline{MINTR2}$	R-2
$\overline{RST}$	B-1	NPADDR3	D-1	BD20	J-16	RACU	R-3
HSREQ0	B-2	NPADDR6	D-2	BD19	J-17	RA6	R-4
HSACK	B-3	NPMODE	D-3	NP7	K-1	RA2	R-5
QCTRL2	B-4	GND	D-15	NP8	K-2	RBCU	R-6
QCTRL0	B-5	BD8	D-16	GND	K-3	GND	R-7
ADDR13	B-6	BD11	D-17	GND	K-15	GND	R-8
ADDR11	B-7	NPADDR0	E-1	BD22	K-16	GND	R-9
ADDR9	B-8	NPADDR2	E-2	BD21	K-17	GND	R-10
ADDR6	B-9	NPADDR5	E-3	NP6	L-1	VCC	R-11
ADDR4	B-10	GND	E-15	NP5	L-2	GND	R-12
ADDR2	B-11	BD10	E-16	NP4	L-3	X3	R-13
ADDR0	B-12	BD12	E-17	GND	L-15	X0	R-14
$\overline{WR}$	B-13	NP14	F-1	BD24	L-16	XS0	R-15
BDTAG	B-14	BMCLK	F-2	BD23	L-17	BDP2	R-16
BD1	B-15	NPADDR1	F-3	NP3	M-1	BDP0	R-17
BD4	B-16	GND	F-15	NP2	M-2	$\overline{XDAMAT}$	T-1
BD7	B-17	BD13	F-16	NP0	M-3	$\overline{XSAMAT}$	T-2

PGA PIN DESIGNATIONS (Continued)
(Listed by Pin Number)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
RA7	T-3	RS1	T-11	RA5	U-2	RS4	U-10
RA3	T-4	XCU	T-12	RA4	U-3	RS2	U-11
RA0	T-5	X6	T-13	RA1	U-4	RS0	U-12
RB7	T-6	X4	T-14	RBCL	U-5	XCL	U-13
RB5	T-7	X1	T-15	RB6	U-6	X7	U-14
RB3	T-8	XS1	T-16	RB4	U-7	X5	U-15
RB0	T-9	BDP3	T-17	RB2	U-8	X2	U-16
RS3	T-10	RACL	U-1	RB1	U-9	XS2	U-17

PGA PIN DESIGNATIONS
(Listed by Pin Name)

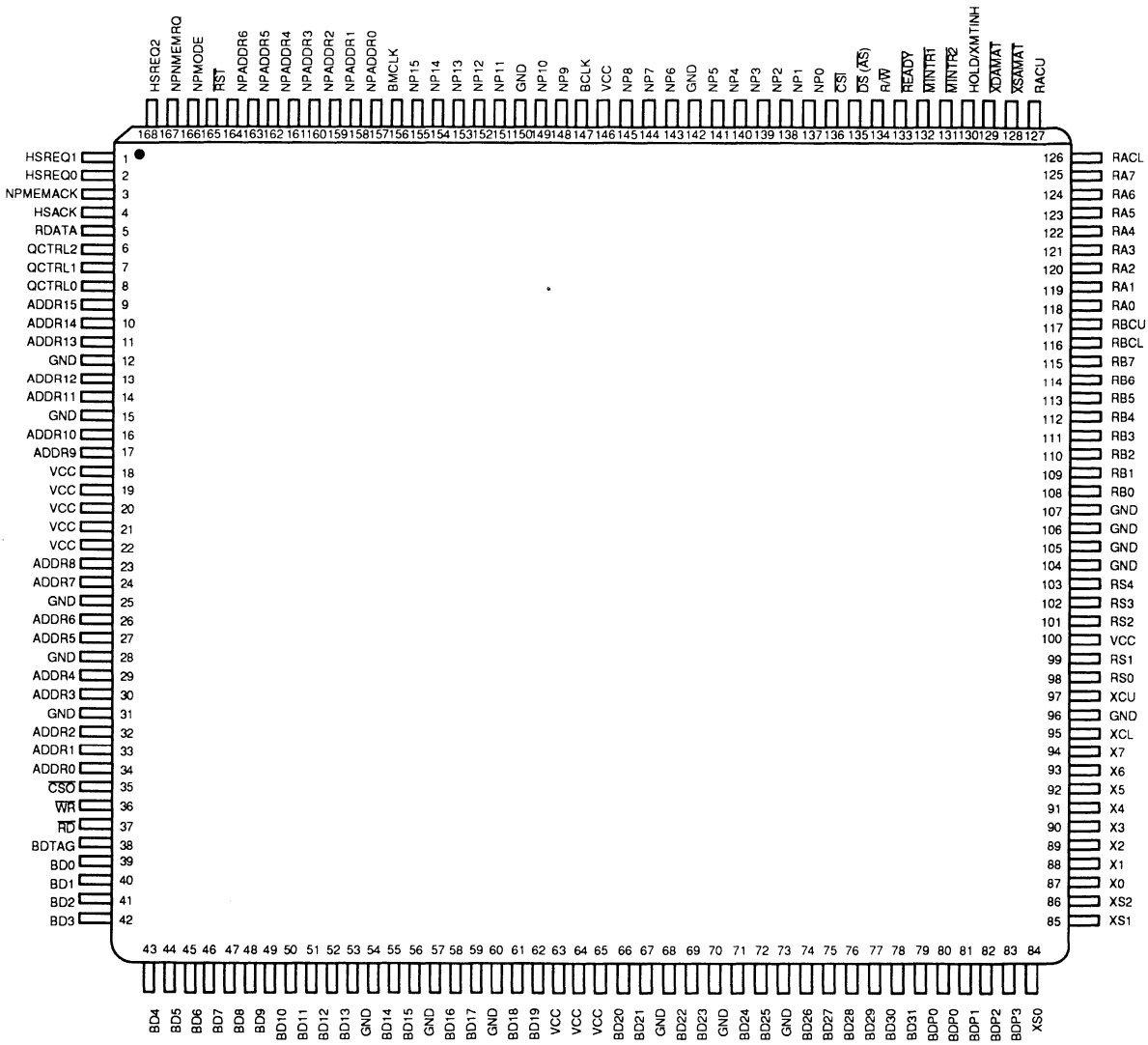
Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
ADDR0	B-12	BD17	H-16	GND	K-15	NPADDR3	D-1
ADDR1	A-12	BD18	H-17	GND	L-15	NPADDR4	C-1
ADDR2	B-11	BD19	J-17	GND	M-15	NPADDR5	E-3
ADDR3	A-11	BD20	J-16	GND	R-7	NPADDR6	D-2
ADDR4	B-10	BD21	K-17	GND	R-8	NPMEMACK	C-4
ADDR5	A-10	BD22	K-16	GND	R-9	NPMEMRQ	C-2
ADDR6	B-9	BD23	L-17	GND	R-10	NPMODE	D-3
ADDR7	A-9	BD24	L-16	GND	R-12	QCTRL0	B-5
ADDR8	A-8	BD25	M-17	HOLD/XMTINH	P-3	QCTRL1	A-3
ADDR9	B-8	BD26	M-16	HSACK	B-3	QCTRL2	B-4
ADDR10	A-7	BD27	N-17	HSREQ0	B-2	RA0	T-5
ADDR11	B-7	BD28	N-16	HSREQ1	C-3	RA1	U-4
ADDR12	A-6	BD29	P-17	HSREQ2	A-1	RA2	R-5
ADDR13	B-6	BD30	N-15	$\overline{\text{MINTR1}}$	R-1	RA3	T-4
ADDR14	A-5	BD31	P-16	$\overline{\text{MINTR2}}$	R-2	RA4	U-3
ADDR15	A-4	BDP0	R-17	NP0	M-3	RA5	U-2
BCLK	J-1	BDP1	P-15	NP1	N-1	RA6	R-4
BD0	A-15	BDP2	R-16	NP2	M-2	RA7	T-3
BD1	B-15	BDP3	T-17	NP3	M-1	RACL	U-1
BD2	A-16	BDTAG	B-14	NP4	L-3	RACU	R-3
BD3	C-15	BMCLK	F-2	NP5	L-2	RB0	T-9
BD4	B-16	$\overline{\text{CSI}}$	N-2	NP6	L-1	RB1	U-9
BD5	A-17	$\overline{\text{CSO}}$	A-13	NP7	K-1	RB2	U-8
BD6	C-16	$\overline{\text{DS}}$ ($\overline{\text{AS}}$)	P-1	NP8	K-2	RB3	T-8
BD7	B-17	GND	C-5	NP9	J-2	RB4	U-7
BD8	D-16	GND	C-6	NP10	H-1	RB5	T-7
BD9	C-17	GND	C-12	NP11	H-2	RB6	U-6
BD10	E-16	GND	C-13	NP12	G-1	RB7	T-6
BD11	D-17	GND	C-14	NP13	G-2	RBCL	U-5
BD12	E-17	GND	D-15	NP14	F-1	RBCU	R-6
BD13	F-16	GND	E-15	NP15	G-3	RDATA	A-2
BD14	F-17	GND	F-15	NPADDR0	E-1	$\overline{\text{RD}}$	A-14
BD15	G-16	GND	H-3	NPADDR1	F-3	$\overline{\text{READY}}$	N-3
BD16	G-17	GND	K-3	NPADDR2	E-2	RS0	U-12

PGA PIN DESIGNATIONS (Continued)
(Listed by Pin Name)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
RS1	T-11	**VCC**	C-9	**$\overline{WR}$**	B-13	**X7**	U-14
RS2	U-11	**VCC**	C-10	**X0**	R-14	**XCL**	U-13
RS3	T-10	**VCC**	C-11	**X1**	T-15	**XCU**	T-12
RS4	U-10	**VCC**	G-15	**X2**	U-16	**$\overline{XDAMAT}$**	T-1
$\overline{RST}$	B-1	**VCC**	H-15	**X3**	R-13	**XS0**	R-15
R/$\overline{W}$	P-2	**VCC**	J-3	**X4**	T-14	**XS1**	T-16
VCC	C-7	**VCC**	J-15	**X5**	U-15	**XS2**	U-17
VCC	C-8	**VCC**	R-11	**X6**	T-13	**$\overline{XSAMAT}$**	T-2

CONNECTION DIAGRAM

168-Pin PQFP (Top View)



14977-039A

PQFP PIN DESIGNATIONS
(Listed by Pin Number)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
HSREQ1	1	$\overline{CSO}$	35	BD23	69	RS4	103
HSREQ0	2	$\overline{WR}$	36	GND	70	GND	104
NPMEMACK	3	$\overline{RD}$	37	BD24	71	GND	105
HSACK	4	BDTAG	38	BD25	72	GND	106
RDATA	5	BD0	39	GND	73	GND	107
QCTRL2	6	BD1	40	BD26	74	RB0	108
QCTRL1	7	BD2	41	BD27	75	RB1	109
QCTRL0	8	BD3	42	BD28	76	RB2	110
ADDR15	9	BD4	43	BD29	77	RB3	111
ADDR14	10	BD5	44	BD30	78	RB4	112
ADDR13	11	BD6	45	BD31	79	RB5	113
GND	12	BD7	46	BDP0	80	RB6	114
ADDR12	13	BD8	47	BDP1	81	RB7	115
ADDR11	14	BD9	48	BDP2	82	RBCL	116
GND	15	BD10	49	BDP3	83	RBCU	117
ADDR10	16	BD11	50	XS0	84	RA0	118
ADDR9	17	BD12	51	XS1	85	RA1	119
VCC	18	BD13	52	XS2	86	RA2	120
VCC	19	GND	53	X0	87	RA3	121
VCC	20	BD14	54	X1	88	RA4	122
VCC	21	BD15	55	X2	89	RA5	123
VCC	22	GND	56	X3	90	RA6	124
ADDR8	23	BD16	57	X4	91	RA7	125
ADDR7	24	BD17	58	X5	92	RACL	126
GND	25	GND	59	X6	93	RACU	127
ADDR6	26	BD18	60	X7	94	$\overline{XSAMAT}$	128
ADDR5	27	BD19	61	XCL	95	$\overline{XDAMAT}$	129
GND	28	VCC	62	GND	96	HOLD/XMTINH	130
ADDR4	29	VCC	63	XCU	97	$\overline{MINTR2}$	131
ADDR3	30	VCC	64	RS0	98	$\overline{MINTR1}$	132
GND	31	BD20	65	RS1	99	$\overline{READY}$	133
ADDR2	32	BD21	66	VCC	100	R/$\overline{W}$	134
ADDR1	33	GND	67	RS2	101	$\overline{DS}$ ($\overline{AS}$)	135
ADDR0	34	BD22	68	RS3	102	$\overline{CSI}$	136

PQFP PIN DESIGNATIONS
(Listed by Pin Number)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
NP0	137	NP7	145	NP12	153	NPADDR3	161
NP1	138	NP8	146	NP13	154	NPADDR4	162
NP2	139	VCC	147	NP14	155	NPADDR5	163
NP3	140	BCLK	148	NP15	156	NPADDR6	164
NP4	141	NP9	149	BMCLK	157	$\overline{RST}$	165
NP5	142	NP10	150	NPADDR0	158	NPMODE	166
GND	143	GND	151	NPADDR1	159	NPMEMRQ	167
NP6	144	NP11	152	NPADDR2	160	HSREQ2	168

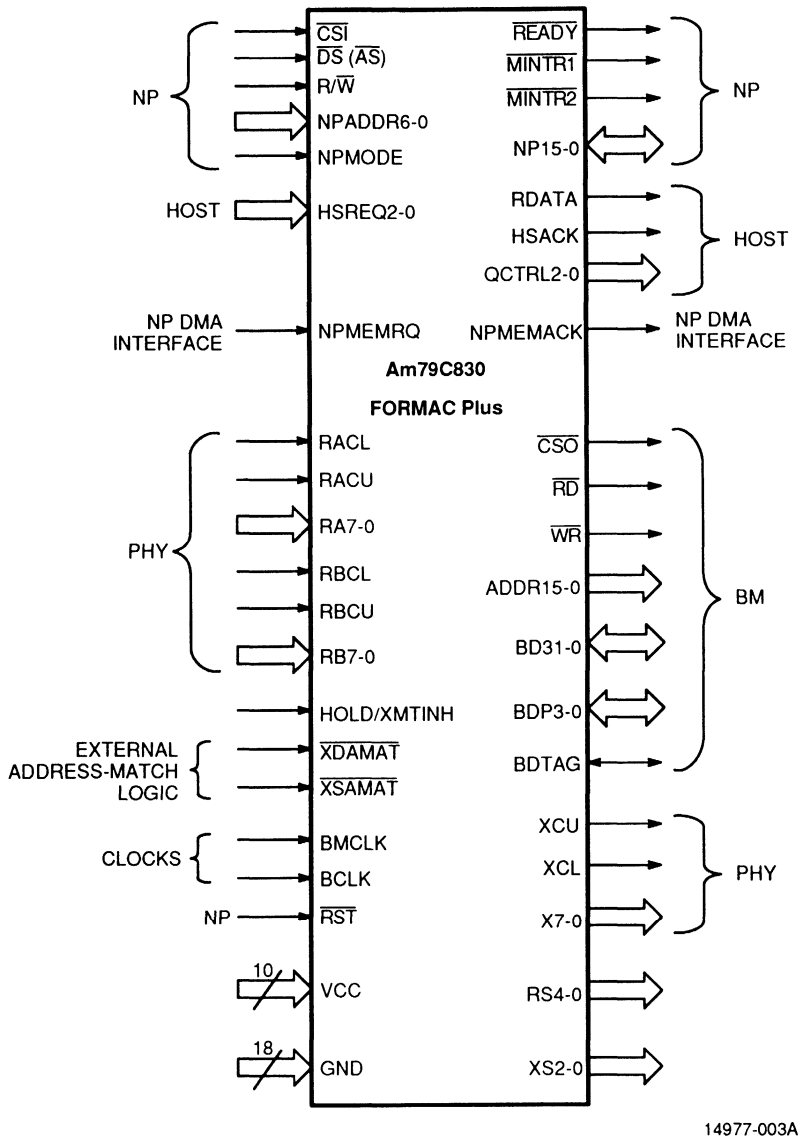
PQFP PIN DESIGNATIONS
(Listed by Pin Name)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
ADDR0	34	BD17	58	GND	73	NPADDR3	161
ADDR1	33	BD18	60	GND	96	NPADDR4	162
ADDR2	32	BD19	61	GND	104	NPADDR5	163
ADDR3	30	BD20	65	GND	105	NPADDR6	164
ADDR4	29	BD21	66	GND	106	NPMEMACK	3
ADDR5	27	BD22	68	GND	107	NPMEMRQ	167
ADDR6	26	BD23	69	GND	143	NPMODE	166
ADDR7	24	BD24	71	GND	151	QCTRL0	8
ADDR8	23	BD25	72	HOLD/XMTINH	130	QCTRL1	7
ADDR9	17	BD26	74	HSACK	4	QCTRL2	6
ADDR10	16	BD27	75	HSREQ0	2	RA0	118
ADDR11	14	BD28	76	HSREQ1	1	RA1	119
ADDR12	13	BD29	77	HSREQ2	168	RA2	120
ADDR13	11	BD30	78	$\overline{\text{MINTR1}}$	132	RA3	121
ADDR14	10	BD31	79	$\overline{\text{MINTR2}}$	131	RA4	122
ADDR15	9	BDP0	80	NP0	137	RA5	123
BCLK	148	BDP1	81	NP1	138	RA6	124
BD0	39	BDP2	82	NP2	139	RA7	125
BD1	40	BDP3	83	NP3	140	RACL	126
BD2	41	BDTAG	38	NP4	141	RACU	127
BD3	42	BMCLK	157	NP5	142	RB0	108
BD4	43	$\overline{\text{CSI}}$	136	NP6	144	RB1	109
BD5	44	$\overline{\text{CSO}}$	35	NP7	145	RB2	110
BD6	45	$\overline{\text{DS}}$ ($\overline{\text{AS}}$)	135	NP8	146	RB3	111
BD7	46	GND	12	NP9	149	RB4	112
BD8	47	GND	15	NP10	150	RB5	113
BD9	48	GND	25	NP11	152	RB6	114
BD10	49	GND	28	NP12	153	RB7	115
BD11	50	GND	31	NP13	154	RBCL	116
BD12	51	GND	53	NP14	155	RBCU	117
BD13	52	GND	56	NP15	156	$\overline{\text{RD}}$	37
BD14	54	GND	59	NPADDR0	158	RDATA	5
BD15	55	GND	67	NPADDR1	159	$\overline{\text{READY}}$	133
BD16	57	GND	70	NPADDR2	160	RS0	98

PQFP PIN DESIGNATIONS
(Listed by Pin Name)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
RS1	99	VCC	20	$\overline{WR}$	36	X7	94
RS2	101	VCC	21	X0	87	XCL	95
RS3	102	VCC	22	X1	88	XCU	97
RS4	103	VCC	62	X2	89	$\overline{XDAMAT}$	129
$\overline{RST}$	165	VCC	63	X3	90	XS0	84
R/$\overline{W}$	134	VCC	64	X4	91	XS1	85
VCC	18	VCC	100	X5	92	XS2	86
VCC	19	VCC	147	X6	93	$\overline{XSAMAT}$	128

LOGIC SYMBOL



14977-003A

Legend:

NP – NODE PROCESSOR

PHY – PHYSICAL LAYER

BM – BUFFER MEMORY

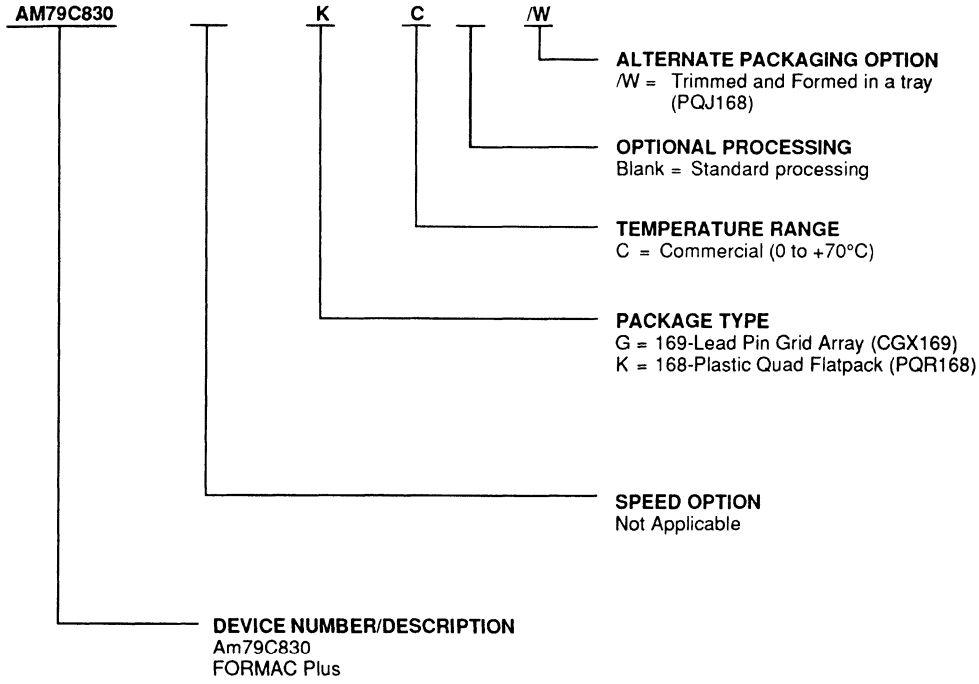
VCC – +5 VOLTS

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of these elements:

Device Number
Speed Option (if applicable)
Package Type
Temperature Range
Optional Processing
Alternate Packaging Option



Valid Combinations	
AM79C830	GC, KC, KC/W

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

Physical-Layer (PHY) Interface (30 pins)

The following section describes the pins that interface the FORMAC Plus with the physical layer (PHY) device. These signals are synchronous to BCLK.

RACU

Receive A Control Upper (input)

RACU is asserted high to indicate that the upper nibble of the RA bus (RA7-4) is a network control character. When RACU is low, this nibble contains data. RACU is synchronous to BCLK.

RACL

Receive A Control Lower (input)

RACL is asserted high to indicate that the lower nibble of the RA bus (RA3-0) is a network control character. When RACL is low, this nibble contains data. RACL is synchronous to BCLK.

RA7-0

Receive Bus A (input)

The RA bus is used to receive information from the physical layer (PHY) device. Bytes clocked from the physical layer (PHY) into the FORMAC Plus RA bus input are synchronous to BCLK.

RBCU

Receive B Control Upper (input)

RBCU is asserted high to indicate that the upper nibble of the RB bus (RB7-4) is a network control character. When RBCU is low, this nibble contains data. RBCU is synchronous to BCLK.

RBCL

Receive B Control Lower (input)

RBCL is asserted high to indicate that the lower nibble of the RB bus (RB3-0) is a network control character. When RBCL is low, this nibble contains data. RBCL is synchronous to BCLK.

RB7-0

Receive Bus B (input)

The RB-bus is used to receive information from the physical layer (PHY) device. Bytes clocked from the physical layer (PHY) into the FORMAC Plus RB bus input are synchronous to BCLK.

XCU

Transmit Control Upper (output)

The XCU output signal is used to flag control symbols being presented on the upper nibble of the transmit bus. This signal is synchronous to BCLK. If XCU is asserted high, the upper nibble of the X bus is interpreted as a network control character. Otherwise, it is interpreted as a data nibble.

XCL

Transmit Control Lower (output)

The XCL output signal is used to flag control symbols being presented on the lower nibble of the transmit bus. This signal is synchronous to BCLK. If XCL is asserted high, the lower nibble of the X bus is interpreted as a network control character. Otherwise, it is interpreted as a data nibble.

X7-0

Transmit Bus (output)

This eight-bit output bus is used to send control and data information to the physical layer (PHY) device to be transmitted over the medium. Information on the X bus output is synchronous to BCLK.

Node-Processor (NP) interface (30 pins)

The following paragraphs describe the pins used to interface the FORMAC Plus with the node processor (NP) or other control devices. The NP interface is used for initializing the FORMAC Plus as well as for reporting status.

$\overline{\text{CSI}}$

Chip Select Input (input)

– Asynchronous when NPMODE = 0

– Synchronous when NPMODE = 1

The chip-select Input (active low) enables Read and Write operations to the FORMAC Plus. In the asynchronous mode, the data output is enabled while $\overline{\text{CSI}}$ and $\overline{\text{DS}}$ are both low and R/$\overline{\text{W}}$ is high. In the synchronous mode, the data output is enabled while $\overline{\text{CSI}}$ is low and R/$\overline{\text{W}}$ is high.

$\overline{DS}$ ($\overline{AS}$)

Data Strobe/Address Strobe (input)

–Asynchronous when NPMODE = 0

–Synchronous when NPMODE = 1

The $\overline{DS}$ input (active low) is used in the handshake between the NP and FORMAC Plus when the FORMAC Plus acts as bus slave during register accesses. In the asynchronous mode, this input signal is set by the node processor to transfer data between the NP and the FORMAC Plus. The direction of the data transfer is dictated by the logic level of the R/$\overline{W}$ line. The NP sets $\overline{DS}$ low to initiate a data transfer. In the synchronous mode, $\overline{DS}$ functions as an address strobe ($\overline{AS}$) and is used in conjunction with BCLK to latch the NPADDR bus (see Figure 2). In either mode, the chip-select input ($\overline{CSI}$) must be low while $\overline{DS}$ is low in order to start an NP bus transaction.

NPADDR6-0

NP Address bus (input)

The NPADDR6-0 input lines allow direct access to FORMAC Plus internal registers. In addition, these lines are used to place FORMAC Plus into different operating states.

The NPADDR bus of the FORMAC Plus performs two control functions. First, the input on NPADDR6-0 acts as an address, selecting the proper internal register for a read or write operation that is controlled by the R/$\overline{W}$ pin. The data is either read onto or loaded from the 16-bit NP bus. For a discussion of the results of read and load instructions, see the section under Programming the FORMAC Plus. Secondly, using the NPADDR bus, instructions or commands can be issued to FORMAC Plus.

NP15-0

NP Data Bus (input, output, high impedance)

The NP bus is a 16-bit wide bidirectional data bus used to interface the FORMAC Plus to the node processor. Data transfer on the NP bus can be synchronous or asynchronous depending upon the setting of the NPMODE pin. For asynchronous operation, a two-wire handshake is provided through the $\overline{READY}$ and data-strobe ($\overline{DS}$) lines.

NPMODE

NP Bus Mode (input)

The level on the NPMODE pin defines the type of NP-bus interface with the FORMAC Plus. When NPMODE is strapped high, the NP interface operates synchronously with BCLK. When NPMODE is strapped low, asynchronous interface operation is selected.

$\overline{MINTR1}$

Maskable Interrupt 1 (output, open drain)

The $\overline{MINTR1}$ output (active low) is an attention line to the NP. $\overline{MINTR1}$, when active, indicates an interrupt due to one or more unmasked flags in status register 1. In general, the active state of $\overline{MINTR1}$ indicates that an unmasked interrupt condition or a transmit condition has occurred. $\overline{MINTR1}$ is deactivated once either the lower or upper 16 bits of status register 1 (ST1L or ST1U) are read. Once $\overline{MINTR1}$ is asserted, all 32 bits of status register 1 must be read to enable any future interrupt on this pin.

$\overline{MINTR2}$

Maskable Interrupt 2 (output, open drain)

The $\overline{MINTR2}$ output (active low) is an attention line to the NP. $\overline{MINTR2}$, when active, indicates an interrupt due to one or more unmasked flags in status register 2. In general, the active state of $\overline{MINTR2}$ indicates that an unmasked interrupt condition, a receive condition, or a change in ring status has occurred. $\overline{MINTR2}$ is deactivated once either the lower or upper 16 bits of status register 2 (ST2L or ST2U)are read. Once $\overline{MINTR2}$ is asserted, all 32 bits of status register 2 must be read in order to enable any future interrupt on this pin.

$\overline{READY}$

Ready (output, open drain)

In asynchronous mode, the $\overline{READY}$ output (active low) is used in the handshake between the NP and FORMAC Plus. The FORMAC Plus $\overline{READY}$ output provides an asynchronous acknowledgment to the NP that data transfer is complete. The FORMAC Plus asserts $\overline{READY}$ when it has put the data onto the NP bus during a read cycle, or when it has taken the data from the NP bus during a write cycle. $\overline{READY}$ is a response to the $\overline{CSI}$ and $\overline{DS}$, and returns high after the $\overline{CSI}$ or $\overline{DS}$ signal goes high.

In the synchronous mode, the $\overline{READY}$ line goes active on the BCLK edge when $\overline{CSI}$ and $\overline{DS}$ are active. $\overline{READY}$ goes inactive on the following BCLK edge. In the case of loading/reading of the MDR (memory data register), $\overline{READY}$ goes active on the BCLK edge after the completion of any pending data transfer from/to buffer memory.

R/$\overline{W}$

Read or $\overline{W}$rite select (input)

The R/$\overline{W}$ line is used to select the type of access (i.e. read or write) between the FORMAC Plus and the NP. If R/$\overline{W}$ is high, data is read from the FORMAC Plus to the NP. If R/$\overline{W}$ is low, the data flow is from the NP to the FORMAC Plus.

Buffer-Memory Interface (56 Pins)

ADDR15-0

Buffer Memory Address (output, high impedance)

The 16-bit ADDR-bus provides the addresses that access the buffer memory. The address selection depends on the result of bus arbitration in the FORMAC Plus. Each memory access lasts for two BMCLK clock cycles and the address is valid for both of these cycles. When buffer memory control has been released to the NP, the ADDR bus is in the high-impedance state.

Note: As long as the use of the buffer memory has not been granted to the node processor or host (HSACK and NPMEMACK not active), the FORMAC Plus may drive the address lines even though no control signals are active.

BD31-0

Buffer Memory Data Bus (input, output, high impedance)

The 32-bit BD bus interfaces the FORMAC Plus to the buffer memory or any external logic using this bus. These lines transfer data to and from the buffer memory for the FORMAC Plus. These signals are synchronous to BMCLK.

BDP3-0

Buffer Data Parity Bus (input, output, high impedance)

The BDP3-0 bus contains the four byte-parity lines for the BD bus, in both the nontag and tag modes, as shown in the following table:

BD-Bus Lines	Corresponding Parity Lines
BD7-0 and tag bit (tag mode only)	BDP0
BD15-8	BDP1
BD23-16	BDP2
BD31-24	BDP3

Note:
BD bus parity can be either even or odd, based on the state of the parity bit (bit 12) in mode register 2 (MDREG2).

BDTAG

Tag Mode Only (input, output, high impedance)

In receive mode, this bit defines whether the information on the BD bus is data (BDTAG = 0) or frame status (BDTAG = 1). In transmit mode, when BDTAG = 1, it indicates that the end of a frame has been reached, as indicated by the presence of a tag bit in both the last long word and the descriptor word at the end of the frame. In transmit mode, when BDTAG = 0, it indicates that the information on the BD bus is data, i.e. end-of-frame not yet reached.

$\overline{\text{CSO}}$

Chip-Select Output (output, high impedance)

The chip-select output (active low) is a select signal for buffer memory read and write operations. This line is in the high-impedance state when buffer memory control is released to the NP.

$\overline{\text{RD}}$

Buffer Memory Read (output, high impedance)

This output signal (active low) controls the buffer memory during a buffer-memory read accesses. This line is in the high-impedance state when buffer memory control is released to the NP.

$\overline{\text{WR}}$

Buffer Memory Write (output, high impedance)

This (active low) output signal, in its active-low state, allows write accesses to buffer memory. This line is in the high-impedance state when buffer memory control is released to the NP.

Host/Buffer-Memory Interface (8 pins)

All these signals are synchronous to BMCLK.

HSACK

Host Acknowledge (output)

This signal indicates that the current host read/write request is being granted by FORMAC Plus and allows read/write accesses of buffer memory by the host.

HSREQ2-0

Host Request Bus (input)

The host request bus specifies to FORMAC Plus the type of buffer memory access the host requires, as described in Table 1.

Special-frame write requests are used to set up claim, beacon, and auto-void frames in the buffer memory. (see the discussion under Buffer Memory Operation). These requests make use of the WPXSF register to set up special frames in the special-frame area.

Read request is used to retrieve received frames from buffer memory and store them in the system memory. Write requests are used to set up frames in buffer memory for transmission.

Table 1. Encoding of the Host Request bus (HSREQ2–0).

HSREQ2	HSREQ1	HSREQ0	Type of Request
0	0	0	None.
0	0	1	Reserved.
0	1	0	Special Frame Write Request.
0	1	1	Read Request: Receive Queue.
1	0	0	Write Request: Synchronous Queue.
1	0	1	Write Request: Asynchronous Queue 0.
1	1	0	Write Request: Asynchronous Queue 1.
1	1	1	Write Request: Asynchronous Queue 2.

QCTRL2-0

Buffer Queue Control (output)

These three status output lines are encoded as described in Table 2.

These signals communicate to the host the current condition of the transmit queues. The meanings of these states are as follows:

a. Quiescent; or space remains for more data while loading a transmit queue.

The quiescent state exists when FORMAC Plus is neither transmitting nor receiving. This queue-status message is also sent to the host while loading a buffer-memory transmit queue (and not yet reading out of the queue) and space remains for more data.

b. Request transfer into Synchronous queue; Asynchronous queue 0; Asynchronous queue 1; or Asynchronous queue 2.

These signals are sent to the host as long as the corresponding queue is not yet in the almost full state and, at the same time, the FORMAC Plus is reading out of the queue. The host can transfer more data into this queue on receiving any of these signals.

These are level signals and remain in this state as long as this condition exists.

c. Abort this transmit frame

This queue-status message is given to the host when all of the following three conditions are satisfied:

1. The host has issued a write request for this queue
2. Transmit FIFO underrun occurs
3. Transmit buffer-memory underrun occurs for this queue.

This signal condition is asserted for one clock cycle only.

d. Current Queue Almost Full

This queue-status message is sent to the host to indicate that the number of free long words remaining in the transmit queue being written to has decreased to the almost-full value (AFULL3-0) programmed in mode register 2. This signal condition is asserted for one clock cycle.

Note: If AFULL3-0 is set to 0000, no current-queue-almost-full message is produced, even when the transmit FIFO in buffer memory is full.

Table 2. Encoding of the Buffer Queue Control (QCTRL2–0) pins.

QCTRL2	QCTRL1	QCTRL0	Meaning(s)
0	0	0	(1) Quiescent. (2) Space remains for more data while loading a transmit queue.
0	0	1	Request transfer into Synchronous Queue.
0	1	0	Request transfer into Asynchronous Queue 0.
0	1	1	Request transfer into Asynchronous Queue 1.
1	0	0	Request transfer into Asynchronous Queue 2.
1	0	1	Abort this transmit frame.
1	1	0	Reserved.
1	1	1	Current queue almost full.

RDATA

Receive Data (output)

This signal indicates that received data is present in the buffer memory and is ready to be transferred by the host to system memory. Read requests are not acknowledged when RDATA is inactive. This signal is valid in tag mode only.

NP/Buffer-Memory Interface (2 pins)

NPMEMRQ

Node Processor Memory Request (input)

The input signal NPMEMRQ is a request by the node processor to obtain control of buffer memory.

NPMEMACK

Node Processor Memory Access Acknowledge (output)

This signal indicates that an NPMEMRQ has been granted and that the NP now has control of buffer memory (ADDR-bus, $\overline{RD}$, $\overline{WR}$, $\overline{CSO}$, BDP, BD, and BDTAG). If NPMEMACK is forced low while NPMEMRQ is active (due to a higher priority request), the NP must release control of the bus within two BMCLK periods after the NPMEMACK line goes inactive.

Special-Functions (11 pins)

HOLD/XMTINH

Hold/Transmit Inhibit (input)

HOLD acts as a suspend/resume feature. On asserting this signal high, FORMAC Plus freezes the states of the transmit and receive state machines, and the TRT, THT, TMSYNC and TVX timers. Once this signal is de-asserted operation is resumed on the next BCLK. XMTINH can be used to inhibit transmission even if the conditions for transmission are valid.

This pin can be programmed for a transmit-inhibit function or a hold function by appropriately setting the XMTINH/HOLD bit in mode register 1. See the discussion of On-Line Mode, and Mode Register 1.

RS4-0

Receive Status (output)

The receive-status (RS4-0) pins indicate the type of frame received, and the condition of the receive state machine. These status output pins are encoded as illustrated in Table 3.

Table 3. Encoding of the Receive Status (RS4–0) pins.

RS4	RS3	RS2	RS1	RS0	Description
0	0	0	0	0	Quiescent state. No status generated.
0	0	0	0	1	Claim-Frame received.
0	0	0	1	0	Beacon-Frame received.
0	0	0	1	1	Void-Frame received.
0	0	1	0	0	LLC Frame received.
0	0	1	0	1	SMT Frame received.
0	0	1	1	0	Implementor-Frame received.
0	0	1	1	1	Reserved.
0	1	0	X	X	SD Received (Short Address).
0	1	1	X	X	SD Received (Long Address).
1	0	E	A	C	Own frame received and an S or R symbol is present in the E, A, and C indicators of the frame-status area.
1	1	0	0	0	Pass Token – Nonrestricted.
1	1	0	0	1	Pass Token – Restricted.
1	1	0	1	0	Capture Token – Nonrestricted.
1	1	0	1	1	Capture Token – Restricted.
1	1	1	0	0	Ring Operational.
1	1	1	0	1	Ring not Operational.
1	1	1	1	0	Missed Frame.
1	1	1	1	1	Reserved.

Legend:

X = Don't care.

E, A, and C here have either a 1 or 0 value, depending upon the actual set/reset status, respectively, of the E, A, and C indicators in the receive frame.

Note:

All of these status conditions, other than the quiescent state, are asserted for only one BCLK cycle.

The states shown in this table have the following meanings:

a. Quiescent State

This state is entered after reset. While these pins are in the 00000 state, no status is generated by FORMAC Plus.

b. Claim-, Beacon-, Void-, LLC-, SMT-, or Implementor-frame types received.

These status conditions indicate the type of frame received. The received frame must be valid, with an R (reset) in its E frame-status indicator. Frame status is indicated in the second BCLK cycle after receiving the byte containing the end delimiter (T symbol) of the received frame.

c. Start Delimiter (SD) Received with Short Address

This output is provided when the start delimiter (JK) is received and the frame being received has a short address. This output is asserted in the second BCLK cycle following the start delimiter (JK).

d. Start Delimiter (SD) received with Long address

This output is provided when the start delimiter (JK) is received and the frame being received has a long address. This output is asserted in the second BCLK cycle following the start delimiter (JK).

e. Own frame received, with frame-status indicated

This status signal is provided when a frame is received whose source address equals this station's 16-bit or 48-bit address ("my address"), i.e. SA = MA. The error-, address- and frame-copied status of the frame are indicated by an S (set) or R (reset) in the E, A, and C indicators. On the RS2, RS1, and RS0 lines, the set or reset status of each indicator is denoted by a 1 or 0, respectively. These signals are asserted in the clock cycle immediately after the frame-type status is presented (see b. above), i.e. in the third BCLK cycle after the end delimiter is received.

The E line (RS2) is set low if the error-detected indicator (E) is received as reset (R), and is set high if the error-detected indicator received is not reset.

The A line (RS1) is set high if address-recognized indicator (A) received is set (S), and is set low if the indicator is received as reset (R).

The C line (RS0) is set high if frame-copied indicator (C) received is set (S), and set low if the indicator is received as reset (R).

Exception: If either the address-recognized indicator (A) or the frame-copied indicator (C) received is neither set (S) nor reset (R), then the A line (RS1) is set low and the C line (RS0) is set high.

Note: A "my-frame-received" signal can be created in two clock cycles by first decoding the RS4-0 lines for frame type (see b, above), and then, on the second clock, decoding for "own frame received" (as in this step) and neglecting the status of E, A, and C. (i.e. decoding lines RS4 and RS3 only).

f. Pass Token – Nonrestricted

Indicates that a nonrestricted token is received on the RA or RB bus and is being repeated on the X-bus. This status is asserted in the third clock cycle following the byte containing the end delimiter of the token on the RA or RB bus.

g. Pass Token – Restricted

Indicates that a restricted token is received on the RA or RB bus and is being repeated on the X-bus. This status is asserted in the third clock cycle following the byte containing the end delimiter of the token on the RA or RB bus.

h. Capture Token – Nonrestricted

Indicates that a nonrestricted token is received on the RA or RB bus and is being captured. This status is asserted in the third clock cycle following the byte containing the end delimiter of the token on the RA or RB bus.

i. Capture Token – Restricted

Indicates that a restricted token is received on the RA or RB bus and is being captured. This status is asserted in the third clock cycle following the byte containing the end delimiter of the token on the RA or RB bus .

j. Ring Operational

This output combination is provided when the current status of the ring changes from not-operational to operational, as defined by FDDI standards. If this transition occurs at the same time as any other status change, then ring-operational status is given lesser priority. It is then provided in the clock cycle following any other status signal on the RS4-0 pins.

k. Ring Not Operational

This output combination is provided when the current status of the ring changes from operational to not-operational, as defined by FDDI standards. If this transition occurs at the same time as any other status change, then ring-not-operational status is given lesser priority, and is then provided in the clock cycle following any other status signal on the RS4-0 pins.

l. Missed Frame

Whenever an internal or external destination-address match occurs and the received frame could not be copied into buffer memory, then this status is asserted on the RS4-0 pins in the clock cycle following that in which frame-type status is generated (see paragraph b. on previous page).

$\overline{\text{XDAMAT}}$

External Destination Address Match (input, active low)

This input provides a means for additional destination-address detection external to the FORMAC Plus. This pin should be tied high when external destination-address detection is not used. This input should remain asserted for at least one BCLK cycle, and must be deasserted for at least one BCLK cycle before a subsequent external destination address match is recognized. See the discussion of Special Functions under On-Line Mode.

$\overline{\text{XSAMAT}}$

External Source Address Match (input)

This input provides a means for additional source-address detection external to the FORMAC Plus. This pin should be tied high when external source-address detection is not used. This input should remain asserted for at least one BCLK cycle, and must be deasserted for at least one BCLK cycle before a subsequent external destination address match is recognized. See the discussion of Special Functions under On-Line Mode.

XS2-0

Transmit Status (output)

These three pins indicate the transmit-status conditions of the FORMAC Plus and are valid for one clock cycle. These status signals are not present for repeated or stripped frames. The status conditions indicated by these pins are encoded as described in Table 4.

Note the following explanations:

a. Transmit Aborted

This status message is provided when the data on the X bus is aborted and idles are sent. This output is asserted in the same clock cycle as that in which the idle appears on the X bus following the data.

b. Token Issued

After a token is issued by FORMAC Plus, this status output is asserted in the same clock cycle as that in which the end delimiter appears on the X bus. This status output is not provided if a token is received on the RA or RB bus and simply repeated onto the X bus.

c. Transmitting Synchronous Queue; Asynchronous Queue 0; Asynchronous Queue 1; or Asynchronous Queue 2

These status outputs are asserted in the same clock cycle as that in which the start delimiter (SD) appears on the X bus.

Other Signals (3 pins)

BMCLK

Buffer memory Clock (input)

BMCLK is the clock signal that FORMAC Plus uses for generating the signals to the buffer memory. BMCLK is driven with a clock signal in the range of 12.5 MHz (min) to 25 MHz (max). BMCLK is chosen by the user to match the timing and throughput requirements of the buffer memory. Refer to the discussion of buffer-memory operation for more details regarding the relationship between BMCLK and BCLK for a synchronous NP interface.

BCLK

Byte Clock (input)

The BCLK is the network 12.5 MHz clock that runs the FORMAC Plus media-access logic. Data transmitted and received from the physical-layer (PHY) interface is synchronous to BCLK.

Table 4. Encoding of the Transmit Status (XS2–0) pins.

XS2	XS1	XS0	INDICATED STATUS
0	0	0	Quiescent.
0	0	1	Transmit Aborted.
0	1	0	Token Issued.
0	1	1	Reserved.
1	0	0	Transmitting Synchronous Queue.
1	0	1	Transmitting Asynchronous Queue 0.
1	1	0	Transmitting Asynchronous Queue 1.
1	1	1	Transmitting Asynchronous Queue 2.

$\overline{RST}$

Reset (Input)

The RESET ($\overline{RST}$) signal (active low) is an asynchronous input that initializes the internal FORMAC Plus state machines and registers.

Power and Ground

GND

Ground (Input)

There are eighteen ground (GND) pins on the FORMAC Plus chip. They must all be connected to a common external ground reference.

VCC

+5 Volt Power (Input)

There are ten pins carrying +5-volt power (VCC) on the FORMAC Plus chip. They must all be connected to a +5-volt ±5% source.

INTERFACE DESCRIPTION

PHYSICAL LAYER (PHY) INTERFACE. The RA-, RB-, and X- busses and their associated control lines (see Figure 1) make up the FORMAC Plus interface with the FDDI physical layer (PHY). Each of these three busses includes eight information lines, plus two control lines. The control lines, one for each nibble, indicate to the FORMAC Plus in receive, and to the physical layer in transmit, whether the corresponding nibble contains network control characters or data. The use of two receive busses, RA and RB, permits network operation in the FDDI dual-ring configuration.

NODE PROCESSOR (NP) INTERFACE. The node processor interface includes the following functions:

1. DATA TRANSFER (NP bus). Data for initializing, reading or writing the various registers, timers and pointers in the FORMAC Plus is received over the 16-bit NP bus. Data transfers can be either synchronous or asynchronous to the BCLK used.
2. RESOURCE SELECTION (NPADDR). The 7-bit NPADDR bus allows the node processor to access any FORMAC Plus internal register, such as the Mode-, Status-, Command-, Buffer-Memory-Management, and other registers.
3. INTERRUPTS. The interrupt signals $\overline{\text{MINTR1}}$ or $\overline{\text{MINTR2}}$ (one for each status register) are asserted when FORMAC Plus status changes. The interrupts are selectively maskable.
4. NP/FORMAC Plus HANDSHAKE. The data strobe ($\overline{\text{DS}}$), read/write (R/$\overline{\text{W}}$), chip-select Input ($\overline{\text{CSI}}$) and ready ($\overline{\text{READY}}$) signal-lines support the handshake between the node processor and FORMAC Plus.

BUFFER MEMORY INTERFACE. The buffer memory interface includes the following:

1. 32-BIT DATA BUS (BD). This bus is the path for all data transfers between the FORMAC Plus and the buffer memory. It is also the data path for 32-bit DMA data transfers between the host and buffer memory.
2. DATA-BUS PARITY LINES (BDP). The four BDP lines provide one parity bit for each of the four bytes of the BD bus.
3. BUFFER-MEMORY TAG-BIT LINE (BDTAG). The BDTAG line supplies buffer-memory frame-boundary information when FORMAC Plus is in tag mode.
4. 16-BIT ADDRESS BUS (ADDR). This bus contains the address for all transfers of data into and out of the buffer memory. Each buffer-memory address is generated in response to specific network requests, node-processor requests, or host DMA requests.
5. BUFFER-MEMORY READ, WRITE, AND CHIP-SELECT LINES ($\overline{\text{RD}}$, $\overline{\text{WR}}$, and $\overline{\text{CSO}}$). $\overline{\text{RD}}$ and $\overline{\text{WR}}$ control whether a given data access is to be a read or write. $\overline{\text{CSO}}$ is a chip-select signal that is asserted when a buffer-memory read or write takes place.

HOST INTERFACE. The host processor and the buffer memory communicate via a DMA path. It includes the following functions:

1. HOST REQUEST BUS (HSREQ and HSACK). Using the three-bit encoded HSREQ bus, the host can specify six types of buffer-memory-access requests. When asserted, the HSACK signal indicates that the FORMAC Plus has granted a host read/write access to buffer memory.
2. QUEUE CONTROL BUS (QCTRL). The three-bit QCTRL bus provides the host with queue-state information that enables host access to buffer memory. The QCTRL bits are encoded into six states indicating to the host when it can access a queue that is being filled, when the queue is almost full, and when to abort a transmit frame.
3. RECEIVE DATA PRESENT (RDATA). This signal indicates that received data is present in the buffer memory, and ready to be transferred to the host.

NODE-PROCESSOR-TO-BUFFER-MEMORY INTERFACE. (NPMEMRQ and NPMEMACK). These two signals permit direct NP-to-buffer-memory access. NPMEMRQ is asserted when a buffer-memory request is made by the node processor. When the FORMAC Plus grants the request, NPMEMACK is asserted.

SPECIAL INTERFACE LINES. (RS, XS, $\overline{\text{XSAMAT}}$, $\overline{\text{XDAMAT}}$, and HOLD/XMTINH). For special functions, in conjunction with external hardware, these five signals provide receive- and transmit-status to the host (RS and XS); permit external source and destination address detection ($\overline{\text{XSAMAT}}$ and $\overline{\text{XDAMAT}}$); and to either suspend/resume operation, or to inhibit transmission (HOLD/XMTINH).

FUNCTIONAL DESCRIPTION

Receive Data Path

General

The receive data path (see Figure 1) selects between one of three possible inputs; performs a CRC check of the data integrity of the frame; sets or resets the appropriate frame-status symbols at the end of the frame; and latches the frame to the 8-bit-to-32-bit receive demultiplexer.

Input Multiplexer

The first stage in the receive data path is a three-input multiplexer. Its inputs are the RA or RB data busses from the FDDI physical layer (PHY), or the X (transmit) bus output, as shown in Figure 1. In a dual-ring network configuration, requiring two PHYs, the RA input comes from one PHY and RB comes from the other. In a single-ring topology, the RB input remains unused. The selection of which of these busses is used as the active input to the FORMAC Plus is determined by the state of the SELRA bit in mode register 1. Also, in internal-loopback mode, which is used in self-test, the X-bus transmit output becomes the input to the receive data path. These inputs are summarized as follows:

Condition	Input to Receive Data Path
SELRA = 1	RA bus
SELRA = 0	RB bus
Loopback	X bus

Receive CRC Checker

This logic performs a CRC calculation on the received frame using the FDDI-specified 32-bit Autodin II polynomial. The result is compared with the CRC value in the FCS field of the received frame. If there is a match, the frame is repeated on the ring with the frame-status E indicator (error indicator) unchanged. If the indicators do not match, the E indicator is set by the symbol filter and the frame is repeated. As a programming option, frames received with errors may be flushed, or stored in buffer memory.

Symbol Filter

The symbol filter checks each frame for validity in accordance with FDDI criteria. It then modifies the received frame status in the E, A, and C indicators to reflect the outcome of these checks. The contents of the E indicator denotes frame validity. The A indicator denotes whether there is a match between the destination address (DA) on the frame and this station's own address (designated as "MA", for "My Address", i.e. address of this station). The C indicator denotes whether the frame is copied. The following Table 5 summarizes this. **Note**: The S (set) and R (reset) symbols in the table are either received on the frame or modified by the frame-status logic before the frame is repeated back to the ring.

Table 5. Summary of Frame Status E, A, and C Indicators.

Field	Valid Frame	Not a Valid Frame	Address Match	No Address Match	Address Match is Present and Frame is Copied	Frame Not Copied
E	R	S	–	–	–	–
A	–	–	S	R	–	–
C	–	–	–	–	S	R

Notes:

1. An "address-match" condition is present when any of the following is true:

   DA = SAID (short address, individual; i.e. 16-bit addressing)
   DA = SAGP (short address, group; i.e. 16-bit addressing)
   DA = LAID (long address, individual; i.e. 48-bit addressing)
   DA = LAGP (long address, group; i.e. 48-bit addressing)

2. In all cases, DA must not equal zero.
3. If the address-match is performed external to FORMAC Plus, then $\overline{\text{XDAMAT}}$ is asserted for each address match.
4. The E, A, and C fields are not modified for void frames and implementor frames.

Legend:

R = Reset
S = Set

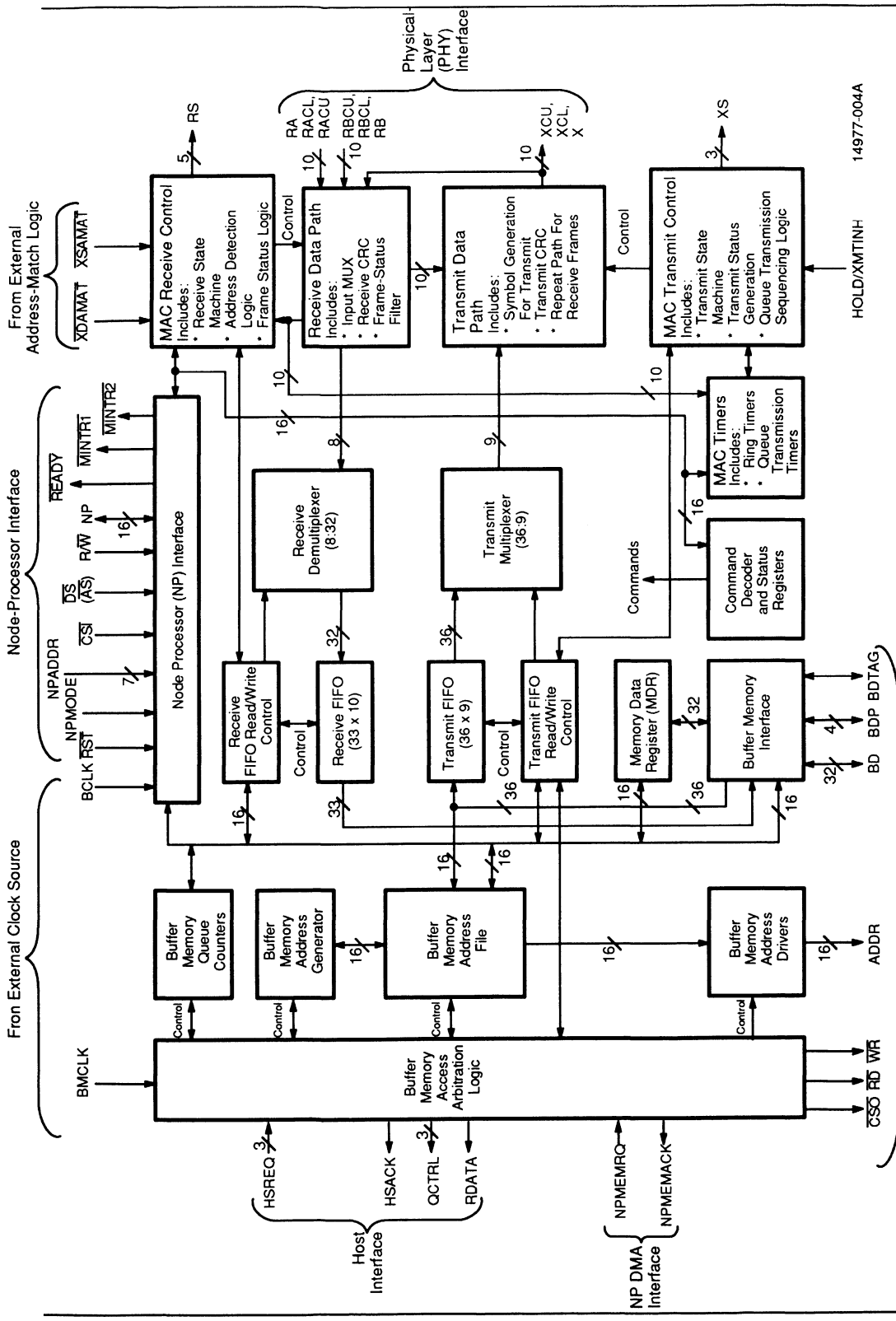


Figure 1. FORMAC Plus Functional Block Diagram

MAC Receive Control

General

The MAC Receive Control contains the receive state-machine, address-detection logic, and frame-status detection and generation logic. It also signals the receive FIFO control circuits when data is present for loading in the receive FIFO.

Receive State-Machine.

The receive state-machine is the control and sequencing logic that implements the various steps in the frame-receive process, as required by the FDDI specification.

Address-Detection Logic

The address-detection logic in the MAC Receive Control compares the source address (SA) and destination address (DA) on each received frame with the 16-bit or 48-bit address of this station (MA). A frame is stripped when the source address on a frame matches the station's own address (i.e. SA = MA). This is how frames are removed once they have circulated around the ring. Normal frame reception occurs when the destination address (DA) of the frame matches the station's address (i.e. DA = MA). In this case, the data from the received frame is loaded into the receive FIFO and the long words are transferred into buffer memory. Note that, as shown in the following table, address detection can also be performed by logic external to the FORMAC Plus. Address detection is summarized as follows:

Condition	Result
SA = MA	Frame stripped
DA = MA	Normal frame reception
$\overline{\text{XSAMAT}}$ asserted	Frame stripped (see Note 1)
$\overline{\text{XDAMAT}}$ asserted	Normal frame reception (see Note 2)

Notes:

1. When SA = MA takes place, using logic external to FORMAC Plus, the $\overline{\text{XSAMAT}}$ input line is asserted.
2. When DA = MA takes place, using logic external to FORMAC Plus, the $\overline{\text{XDAMAT}}$ input line is asserted.

Frame-Status Logic

The frame-status logic verifies the minimum-length requirement of the frame's data field; interprets the contents of the frame control (FC) field in order to determine frame type; and generates various status bits that are used internally as control signals and that are written to a status register for later access.

MAC Timers

General

The Media Access Control (MAC) timer logic (Figure 1) contains the timers and registers required to implement the FDDI timed token protocol.

Timer Logic

The timer logic contains the circuits that control the token claim and beacon process; and the circuits controlling the sequencing of transmission from synchronous and asynchronous queues.

The TRT (token rotation timer) timer counts the time between receipt of tokens. When the ring is operational, the initial value of TRT is the result of the claim process and is stored in the TNEG (negotiated TRT) register. TRT defines how often a station on the ring needs to receive a token. If the time counted by the TRT between the receipt of tokens exceeds the token rotation time currently in use by the network, then the token is considered to be late. If TRT expires twice before a token is received, then network recovery (claim) action is initiated.

Once TTRT is negotiated and a token has been received, synchronous frames (S-frames) can be transmitted until the expiration of a preset synchronous-transmission period. This period is set by the node processor and defines the total amount of synchronous transmission time to be available during any token period.

Synchronous and Asynchronous Queue Timing

Synchronous transmission (i.e., the transmission of S-frames) can take place as soon as a token is captured. When synchronous transmission has terminated (or if there are no S-frames to transmit), the transmission of asynchronous frames (A-frames) can then take place. The time available for asynchronous transmission is measured by the THT (token holding time) counter, which is loaded with the TRT value at the time the token is captured, and starts counting at the completion of synchronous transmission. It continues counting until the token is released. The expiration of THT forces the release of the token after the current frame transmission is complete.

FORMAC Plus maintains three queues for asynchronous transmission. For each of these queues, the node processor assigns a priority value to each queue. This value and the THT value determine the amount of time during which the queue can transmit. When bandwidth is available, FORMAC Plus examines each queue, in

the order: asynchronous queue 0, asynchronous queue 1, and asynchronous queue 2, and compares its priority value to THT. The first queue whose priority value is less than the contents of THT is allowed to transmit. When transmission is complete, the next queue in the sequence is checked. Again, if its priority value is less than that in the THT counter, it can transmit. This sequence continues until either all asynchronous queues have been transmitted or THT has expired, and the token is released.

The TVX (expected time between valid transmissions) timer measures the time between the end–delimiter (ED) fields of frames. The maximum value of TVX is assigned by the node processor via the NP bus. If TVX ever expires, it indicates a ring problem that has interrupted the circulation of both frames and tokens. When this happens, ring recovery is initiated.

Receive Demultiplexer

Received data from a frame is sent via an 8-bit bus to the receive demultiplexer (see Figure 1). The demultiplexer formats four bytes of data into a 32-bit long word, and loads it, a long word at a time, into the receive FIFO. Control of the reading and writing of the demultiplexer is done by the receive FIFO read/write control circuits.

Receive FIFO Read/Write Control

During the reception of data, the MAC receive–control circuits signal the receive FIFO read/write control when the data from a frame is to be stored in the receive FIFO. The receive FIFO read/write control circuits include two state machines: one to control and sequence the writing of data into the receive FIFO, and one to control the reading of data out of the FIFO and into the buffer memory. These circuits also control the loading of the receive demultiplexer, count the length of the data field, and send the requests to the buffer-address arbiter and to the buffer-memory interface to store the data contained in the receive FIFO.

Receive FIFO

The receive FIFO is a 32-bit by 10-word first-in-first-out register that assures continuity of data reception by temporarily storing received data until the buffer memory is ready to receive it. The data-storage format per long word in the FIFO includes an extra bit location that is set to designate the end of each frame, making the actual FIFO format 33 bits by 10.

Buffer Memory Interface

The buffer-memory interface (Figure 1) includes a parity generator for data written to the buffer memory; a parity checker for data read out of the buffer memory; and control circuits for the 32-bit memory data register (MDR) that is used by the node processor when it requires direct communication with the buffer memory. The buffer–memory interface also includes a single output line (BDTAG) for setting the tag bit at the end of a frame in buffer storage (tag-mode only). FORMAC Plus supports odd or even parity per byte, as selected by the host.

Memory Data Register (MDR)

The Memory Data Register (MDR) is a 32-bit holding register used for data transfer between the node processor and buffer memory. The MDR and its associated control circiuts have access to both the 16-bit NP bus and the 32-bit buffer-data (BD) bus. The NP reads data from or writes data to the MDR 16 bits at a time, via the NP bus.

Node Processor (NP) Interface

The node-processor interface is the path for all address, data, control and status communication passing between the FORMAC Plus and the node processor. Node-processor handshake signals include the bidirectional 16-bit data bus, the 7-bit address-bus input, and various control lines. The NP interface-control circuits also include the logic for generating chip-wide resets; the logic for generating interrupts to the node processor; and a register that stores pending MDR requests.

Command Decoder and Status Registers

The Command Decoder and Status Register logic reads and decodes commands and instructions sent to the FORMAC Plus on the 16-bit NP data bus. All instructions are written into one of two command registers (CMDREG1 and CMDREG2). These instructions include such commands as entering or changing various modes of operation, loading the memory data register, clearing or transmitting from specific queues, software reset, etc. The status-register logic allows for status reporting to the node processor via the 16-bit NP bus. This status information can be read out directly or reported using either of the two maskable-interrupt lines $\overline{\text{MINTR1}}$ or $\overline{\text{MINTR2}}$.

Buffer Memory Address File

The buffer-memory address file stores up to thirty 16-bit pointers i.e., addresses. These pointers are involved in the various stages of reading and writing the claim-, beacon-, void-, receive-, synchronous-transmit, and the three levels of asynchronous-transmit queues. Prior to any operation involving buffer memory, the node processor initializes all the pointers for the queues. After initialization, claim and beacon frames are loaded into

buffer memory, and the system can then go into normal on-line mode.

Buffer Memory Address Generator

As data is read into and out of buffer memory, the address of each frame in the queue is read from the address file and incremented by the logic in the address generator. The incremented address is then written back to the address file, thus sequentially developing the address of each frame to be accessed. In this manner, frames are read or written until the last frame of the queue is detected. Queue sizes and end addresses of queues are allocated by the node processor. When the end of a queue is detected by the address-generator logic, the next address wraps back to the start of the queue and reading or writing continues until the end of the data.

Buffer Memory Queue Counters

Introduction

The buffer-memory queue counters work in conjunction with the address-arbitration logic to perform two functions that enhance the movement of data. The first is detection of an almost-full condition in a queue. The second is the use of a threshold level that permits reading of a partial frame in a queue in transmit and receive mode.

Almost-Full Detection

When loading long words into buffer memory to build a transmit queue, the almost-full logic compares the allocated size of the queue to the amount of space remaining as the queue fills. When the amount of space remaining (as measured in free long words) decreases to a predetermined minimum level, an almost-full signal is sent to the host via the three QCTRL lines. The host then uses this information in deciding whether or not to continue loading in order to avoid overflow and the transmission of partial frames.

Threshold Detection

In both transmit and receive modes, when enough long words are assembled in a frame to reach a predetermined threshold, readout of the frame can then take place at the same time that the frame is being written. This reduces the delays associated with waiting for the complete frame. This is valid in tag mode only.

Buffer Memory Access Arbitration Logic

In the course of normal operation, at any given moment the FORMAC Plus must arbitrate between various requests contending for access to buffer memory. Arbitration must be made between requests to transmit queued data; requests to store received data; direct host requests for buffer-memory access; memory-data-register access to buffer memory; and node-processor requests for buffer-memory use. To perform this arbitration, the access-arbitration logic assigns the following priority to each type of request:

Type Of Request	Assigned Priority Level
Transmit	1
Receive	1
Host	2
Memory Data Register (MDR)	3
Node Processor	4

Note that transmit and receive requests are assigned the same priority. When both transmit and receive requests are received, they are serviced in turn; then, on each subsequent request their order of being serviced is reversed.

The access-arbitration logic also controls and sequences the operation of the queue counters, the next-address generation logic, the address file, and the address drivers.

Buffer Memory Address Drivers

Each 16-bit address stored in the buffer-memory address file is transmitted to the external buffer memory via the tristate address drivers.

Transmit FIFO

The transmit FIFO (Figure 1) is a 36-bit by 9-word first-in-first-out register that temporarily stores data to be transmitted. In this way, continuity of data transmission is assured by providing a way to store a portion of the output data stream to compensate for delays involved in accessing the buffer memory. The data-storage format per word in the FIFO includes 32 bits for the four data bytes in each word, plus one parity bit per data byte, i.e. four parity bits per long word, thus making the actual FIFO format 36 by 9.

Transmit FIFO Read/Write Control

The primary purpose of the transmit FIFO read/write control is to provide control for the loading and unloading of the transmit FIFO. The FIFO read/write control also checks the pointers and descriptors that are part of each data frame sent to the FIFO from the buffer memory. If a pointer or descriptor is found to be incorrect, the frame is aborted, transmission of that queue is stopped, and an interrupt is generated. This does not prevent the transmission of other queues. Another function of the transmit FIFO control is to interface with the buffer-

memory access-arbitration logic as part of the transmission process. The transmit-FIFO control also interfaces with the 16-bit node-processor data bus for purposes of control and status functions. The FIFO read/write control logic signals the MAC transmit-control when data is ready to be transferred to the ring.

Transmit Multiplexer

Data to be transmitted is sent from the transmit FIFO to the transmit multiplexer in the form of 32-bit long words (plus parity). The transmit multiplexer reformats each 32-bit long word into a sequence of four 8-bit bytes. These form the input to the transmit data-path logic. The transmit FIFO read/write control circuits sequence the writing in and reading out of this multiplexer. Note that the parity bits are not actually transmitted to the ring, but are used within the FORMAC Plus for special symbol-control purposes.

Transmit Data Path

General

The transmit data path includes a multiplexer that, under state-machine control, selects between data to be transmitted from the transmit multiplexer, and received data that is to be repeated back to the ring, as per FDDI specifications. The transmit data path also includes the logic that adds a CRC value and control symbols to each transmitted frame.

Input to Transmit Path

Depending upon the operating mode in use, the transmit data path selects one of two input sources for the transmitted output to the physical layer (PHY). If the FORMAC Plus is in normal transmit mode, then the transmit data-path input is the byte stream from the transmit multiplexer. When a frame is being repeated, the input to the transmit data-path is the received-data stream, which has been analyzed as to its origin and validity by the MAC receive-control. If a received frame either originated from this station or is defective, as soon as the nature of the frame is determined, the MAC receive-control signals the MAC transmit-control to prevent further repeating of the frame to the ring. All other frames are repeated back to the ring.

Adding CRC to Transmitted Frames

The CRC logic in the transmit data-path computes a 32-bit value from the contents of the frame and then adds this value to the frame-check sequence (FCS) field of the frame, as per FDDI specifications. Note that the FORMAC Plus contains two CRC checking circuits: one for the receive path and one for the transmit path, thus permitting true full-duplex operation.

Adding Control Symbols to Transmitted Frames

The transmit state machine controls the generation of the special symbols that are added to transmit data before being sent out on the ring. The control-symbol-generation logic is part of the transmit data path. These symbols include the idle symbols for the frame preamble; the J and K start-delimiter symbols; the T symbol at the start of the end-delimiter field; and the S and R symbols that designate the set/reset status of the E, A and C indicators at the end of a transmitted or repeated frame. This logic also controls the generation of tokens when they are to be issued.

MAC Transmit Control

The MAC transmit control contains a state machine that operates on two levels. The first-level state machine implements the FDDI MAC transmit protocol. The second level state machine controls the generation of frame symbols and tokens. The MAC transmit control also maintains transmit-status information; controls the restricted-token protocol; and controls idle-symbol transmission so that at least 16 idle symbols are transmitted between frames.

FORMAC Plus OPERATIONAL MODES

Introduction

This section describes the various tasks performed by the FORMAC Plus. FORMAC Plus operation is broken down into five basic modes:

(1) Initialization Mode

(2) Memory-Active Mode

(3) On-Line Mode

(4) On-Line Special Mode

(5) Loopback Mode

Initialization mode is entered after reset. Memory active allows the downloading of frames while the MAC is not on-line. The On-Line mode enables the receive and transmit state machines for operation on the ring. On-Line Special mode is a special case useful in certain applications such as bridge operations. On-Line Special mode does not set the frame-status A indicator nor the frame-status C indicator (valid copy) in the case of an external destination-address match and copy. The two types of loopback mode permit station self-check before entering the on-line state. Selection of these modes is done through mode register 1 (MDREG1).

(1) Initialization Mode

GENERAL. Initialization mode is selected by writing three zeroes in the MMODE bits of MDREG1 (bits 14–12). This mode is automatically entered on a hardware or software reset. In initialization mode, the receive and transmit state machines are locked in the reset condition. The network data path is locked in a 'blind-repeat' configuration in which the data input to the selected receive bus (i.e. RA or RB) is repeated on the X-bus with no protocol processing. **Note:** When entering initialization mode from on-line mode there must be a wait of at least eight BCLK periods before accessing the FORMAC Plus buffer-memory-management registers. This wait is necessary because when changing mode, the FORMAC Plus state machines may be updating the registers, and time must be allowed for the completion of this process.

FORMAC Plus station-address registers can be written only with the chip in initialization mode. Although the timer default values can be written in any mode, the effect on the ring of changing these parameters while on-line should be understood before it is attempted. Network events can occur asynchronous to the loading of the registers. The timers can be loaded with the default at any time. The user, however, cannot determine if the timer is currently operating with the new or old default time.

During Initialization mode, no receiver protocol is executed. When the chip is placed in this mode, certain ring events such as claim or beacon may be missed. Thus, a FORMAC Plus leaving the Initialization mode may not necessarily be operating with current parameters such as the negotiated operative token rotation time for the ring.

TIMERS. Even though the transmit state machine will not process the information, the internal timers, i.e. TRT, THT and TVX, continue to operate. This permits rough timer checkout before going on-line or performing loopback. On reset, TVX is loaded with its terminal count value. This timer expires in 255 clock cycles and status is set accordingly. TVX stops, once expired, until it is reloaded. On reset, TRT is set to 0000 and THT is set to FFFFH. TRT expires in 2exp(21) BCLK cycles. THT stops when the terminal count is reached. Once expired, TRT is reloaded with the current TMAX value and then resumes counting.

COUNTERS. All counters resume sequencing when reloaded. Reloading can be forced by direct writes to the counters. These instructions can be used with the timer expiration bits in the status register to verify timer operation against 'soft' timers during a power-on confidence test of the station hardware. It should also be noted that the timers are loaded with their default values when the MMODE bits of MDREG1 are programmed to exit the initialization mode. For default values of the timers refer to the table: Initialization Values for Timers, Counters, and Related Registers under Programming the FORMAC Plus.

(2) Memory Active Mode

After FORMAC Plus is initialized, the Memory Active mode may be entered to allow the movement of data into the buffer memory. During the Memory Active mode, FORMAC Plus will neither receive frames nor respond to claim or beacon conditions. After the special frames are loaded into buffer memory, the on-line mode may be entered for normal operation.

(3) On-Line Mode

When this mode is entered, FORMAC Plus performs the on-line operational sequences. The chip exits the on-line mode if the MMODE bits are altered or a chip reset occurs.

Receive State

When on-line, the FORMAC Plus continually processes the incoming symbol stream, as per the FDDI receive state-machine. The receive state machine also controls some special-function outputs and counters that are

used to log ring statistics, support external address detection and provide general status information.

Frame Reception

GENERAL. Frame reception is defined as the action of loading network data into the receive FIFO and subsequently into the buffer memory. FORMAC Plus must be in the on-line, on-line-special or loopback modes.

RECEPTION OF FRAME. Normal frame reception can occur in any of the modes selected by the states of the address-detect (ADDET2-0) bits in mode register 1 (MDREG1). In general, when reception occurs, the data from the network is loaded into the receive FIFO, and the long words in the FIFO are transferred to buffer memory. The reception of the end delimiter indicates the end of a frame. Frame status is loaded into buffer memory at the end of the frame in the tag mode, and at the begining of the frame in the nontag mode. Note that token frames, while recognized, used, and repeated, are not "received" since they are not stored.

For frame reception, if all criteria have been met, the state of the transmitter must be considered if the FORMAC Plus is programmed for half-duplex mode. For half-duplex operation the transmitter must be in the idle or repeat state for frame reception. If the FULL/HALF bit is set in MDREG1, the FORMAC Plus is in full duplex mode and may receive frames independent of the transmit state.

Reception does not occur if the receive queue is locked, or if the ADDET2-0 bits in MDREG1 are set to the disable-receive mode.

Received frames can be stored starting at arbitrary byte boundaries using the RXFBB1-0 bits in MDREG2, which act as least significant bit extensions to the WPR pointer. The aligning of frames on a byte boundary is done within FORMAC Plus. Since only long words can be written to the buffer memory, during the first write operation a few of the bytes may be undefined. The start byte boundary cannot be changed on a per-frame basis. Even though there may be undefined bytes in any long words, all bytes/words will have valid parity to prevent generation of parity errors when parity is used.

Frame Flushing

GENERAL. As long as the RCVERR (receive errored frames) bit (bit 4 in MDREG2) is set to 0, frames can be flushed, based on the address-matching or reception-mode criteria selected by the states of the ADDET2-0 bits (bits 10, 9, and 8) in mode register 1 (MDREG1). When a frame is flushed, no references to it are left in buffer memory and the corresponding pointers are restored.

The conditions under which flushing occurs in both tag- and nontag modes are described in the following paragraphs:

(1) Frame Flushing In Tag Mode

CASE A: If RTHR (receive threshold) is not equal to zero, flushing occurs under any of the following conditions:

1. If no internal destination-address match or no external destination-address match ($\overline{\text{XDAMAT}}$) occurs before the end delimiter is received.
2. If the number of long words received on the RA or RB bus *is less than* the value RTHR times 4, and the conditions for receive do not exist.
3. If the number of long words received on the RA or RB bus *exceeds* the value RTHR times 4, and the conditions for receive do not exist, the received frame is aborted in buffer memory by setting the memory-status-receive-abort bit (MSRABT) in the received frame's status word. In this case, the status-receive-abort bit (SRABT) in SR2 is not set.
4. If the frame ends on a nonintegral byte boundary (i.e. the frame contains an odd number of network symbols), in the tag mode, flushing occurs if the number of long words received on the RA or RB bus is less than four times the value of RTHR.

See the discussion of Special Function Operation for other conditions that cause flushing. Also, see the discussion of the address-detect bits ADDET2-0 (MDREG1) for conditions that affect frame flushing.

CASE B: If RTHR (receive threshold) = 0, flushing occurs if no internal destination address match or external destination match ($\overline{\text{XDAMAT}}$) occurs before the end delimiter is received.

(2) Frame Flushing In Nontag Mode

CASE A: If RTHR (receive threshold) is not equal to zero, flushing occurs in any of the following conditions:

1. If no internal destination address match or no external destination address match ($\overline{\text{XDAMAT}}$) occurs before the end delimiter is received
2. If the number of long words received on the RA or RB bus exceeds the value RTHR times 4 and the conditions for receive do not exist.
3. If the frame ends on a nonintegral byte boundary (i.e. the frame contains odd number of network symbols).

See the discussion of Special Functions for other conditions that cause flushing. Also, see the discussion of the address-detect bits ADDET2-0 (MDREG1) for conditions that affect frame flushing.

CASE B: If RTHR = 0, flushing occurs in either of the following two conditions:

1. If no internal destination-address match or external-destination match ($\overline{XDAMAT}$) occurs before the end delimiter is received.
2. If the frame ends on a nonintegral byte boundary (i.e. the frame contains odd number of network symbols)

(3) Frame Flushing of Stripped and Lost Frames

Stripped frames are frames that were partially repeated by a station i.e., the station began to transmit idle (I) symbols before the end delimiter was repeated. The resultant symbol stream is referred to as a stripped frame. A lost frame is one whose symbol stream is corrupted so that a symbol encountered after the start delimiter results in a non-data, non-idle and a non-end-delimiter symbol. In the nontag mode, these frames are flushed.

In the tag mode, these frames are flushed if the number of bytes received does not exceed the receive threshold. If the number of bytes exceeds the receive threshold these frames are flushed if the receive conditions do not exist; otherwise, they are aborted.

Frame Abort

During frame reception, an abort can occur under any of the following conditions:

1) When the receive queue becomes full.
2) If the FORMAC Plus enters a non-repeat, or non-idle transmit state in half-duplex mode.
3) If the disable-receive (DISRCV) condition is programmed in MDREG1, i.e. the ADDET2-0 bits are set to the binary 1 0 0 states, respectively.
4) If the FORMAC Plus is forced out of on-line mode to initialization or memory-active mode.
5) If idle/listen, claim/listen or beacon/listen commands are issued.
6) If the number of long words received on the RA or RB bus in tag mode exceeds four times the RTHR value, and the receive conditions are not satisfied already, abort (rather than flush) occurs.

See the discussion of stripped or lost frames , under Frame Flushing, for other information on frame abort.

FORMAC Plus tolerates an inter-frame gap as small as one byte between two frames on the network. If there is not enough free space in the receive FIFO, then the second frame is aborted, and the MSRABT (memory status receive abort) bit in the receive status word of the second frame is set.

Note: Any length information in the status word of an aborted frame may be inaccurate and should be ignored.

Frame Stripping (non-repeat to ring)

Frames received on the selected RA or RB bus are repeated on the X-bus. In the normal case the entire frame is repeated with the E, A and C frame-status (FS) indicators modified according to the FDDI specification. The FORMAC Plus transmitter can leave the repeat mode for several reasons. When this occurs, the frame received at that time is not repeated and is said to have been stripped.

One primary cause for stripping is the recognition of a frame whose source address (SA) equals the station's own 16-bit or 48-bit address (my address, or MA). This also takes place when $\overline{XSAMAT}$ (external source-address match) is activated. Assertion of $\overline{XSAMAT}$ results in stripping action begining with the byte received on the RA or RB bus at the time of assertion. This is the mechanism for removing frames once they have circulated around the ring. Refer to the paragraphs on special-function operation (below) for a description of stripping action due to external source-address match.

Stripping also occurs when a lost frame is encountered. The byte containing the illegal symbol as well as all subsequent bytes are removed from the ring. Tokens are also stripped when the FORMAC Plus decides to capture one. In this case, only the start delimiter of the token is repeated on the X-bus.

Frame-Status (FS) Handling

The two bytes at the end of each frame (except a token frame) are formatted as follows:

First nibble:
End Delimiter (ED) field contains the symbol T.

Second, third and fourth nibbles:
Frame-Status (FS) indicators. The Frame-Status (FS) indicators contain:

(1) E (error) indicator (second symbol).

(2) A (address-match) indicator (third symbol).

(3) C (frame-copied) indicator (fourth symbol).

The FS indicators at the end of a frame are repeated, stripped or modified according to the FDDI protocol. The first control symbol encountered before the frame-status indicators must be a 'T' in the end-delimiter (ED) field located in the most significant (i.e. upper) nibble on the RA or RB bus. The ED field signifies the end of frame data. Note that if the first control character encountered is misplaced and the 'T' is shifted into the lower nibble of the RA or RB bus, it indicates a problem; i.e. that the frame has an odd number of symbol pairs. When this happens, the byte containing the 'T' and all subsequent indicators are stripped.

The error indicator received should be either set or reset, i.e. it should contain an 'S' or 'R' symbol. If the error indicator is not an 'S' or 'R', an 'S' is assumed. FORMAC Plus recovers the missing error indicator by transmitting an 'S' in the E indicator, and the other indicators are stripped (the 'I' symbol is transmitted). If either the A indicator or C indicator are not 'R' or 'S' symbols, the byte is stripped.

If the frame received is addressed to the station i.e., the internal or external destination-address-match criterion is met and the frame is valid, then the A indicator is set in the repeated frame. If the receive buffer is not full and the frame is copied in the buffer memory, then the C (copied) indicator is set in the repeated frame. If the frame received is not a valid frame (see FDDI standards) then the E indicator is set and the A and C indicators are repeated as received.

Non-Repeated Frames

Frames are not repeated when the FORMAC Plus transmitter is in the transmit-data, issue-token, claim or beacon states, or the send-immediate mode.

Special Functions

The FORMAC Plus receiver processes additional information that is input via certain special-function pins. The following paragraphs explain the special operations performed using these pins:

HOLD/XMTINH OPERATION. If the FORMAC Plus is programmed for HOLD operation (i.e. bit 1 of mode register 1 is low) and the HOLD pin is asserted, it freezes the receive and transmit state machines, and the TRT, THT, TMSYNC and TVX timers. For hold-operation timing, see Figure 35.

When the receive and transmit state machines are on hold, no data bytes are received from the RA or RB bus into the receive FIFO and no data bytes from the transmit FIFO are transmitted to the X-bus. However, transfer from buffer memory into the transmit FIFO and from the receive FIFO take place as appropriate.

When this pin is programmed for XMTINH (i.e. bit 1 of MDREG1 is set high), operation is as follows:

a. If the XMTINH pin is asserted and transmission is not in progress, a new token is not captured.

b. If this pin is asserted while transmission is in progress, the transmission of the current frame is allowed to run to its conclusion, after which a token is issued.

EXTERNAL SOURCE-ADDRESS MATCH ($\overline{\text{XSAMAT}}$). $\overline{\text{XSAMAT}}$ causes the received frame to be stripped from the ring. In reference to external address detection, the $\overline{\text{XSAMAT}}$ input can come as late as the appearance of the end delimiter on the RA or RB bus.

If source-address matching is also being used as a criterion for frame reception (programmed in the MDREG1 register), the $\overline{\text{XSAMAT}}$ should also be correctly asserted to prevent the frame from being flushed. Note the following cases:

CASE 1: If RTHR (receive threshold) is not equal to zero, $\overline{\text{XSAMAT}}$ should be asserted before the number of long words received on RA or RB bus exceeds the value RTHR times 4.

CASE 2: If RTHR is zero, assertion of $\overline{\text{XSAMAT}}$ can come as late as the end delimiter on the RA or RB bus. For external-address timing, see Figure 34.

EXTERNAL DESTINATION ADDRESS MATCH ($\overline{\text{XDAMAT}}$). If destination-address matching is being used as a criterion for frame reception (programmed in the MDREG1 register), the $\overline{\text{XDAMAT}}$ should be correctly asserted to prevent the frame from being flushed and for correct setting of the 'A' frame status indicator. Note the following:

CASE 1: If the receive threshold (RTHR) programmed in FRMTHR is not zero, the $\overline{\text{XDAMAT}}$ must be asserted before the number of long words received on the RA or RB bus exceeds RTHR times 4.

CASE 2: If RTHR is zero, assertion of $\overline{\text{XDAMAT}}$ can come as late as the end delimiter on the RA or RB bus.

$\overline{\text{XDAMAT}}$ should not be asserted before the third clock-cycle following the start delimiter on the RA or RB bus. For external-address timing, see Figure 34.

Transmit State

Introduction

The FORMAC Plus transmitter controls the timing of station transmission as a result of network activity. The operation of the transmitter depends on whether the FORMAC Plus is in normal mode or send-immediate mode.

NORMAL MODE. In the normal mode of operation the transmitter reacts to timer expiration and received MAC frames to queue the claim and beacon frames. The transmitter controls the station's flow of data by enabling data transmission as a result of token capture. The transmitter makes capture and pass decisions based upon the transmit frames queued in tag mode or transmit instructions issued in the nontag mode and token mode (restricted or unrestricted) when the token is received.

Synchronous frames are given priority when conditions indicate that either synchronous or asynchronous frames can be transmitted. When synchronous frames are being transmitted the THT timer is held. This keeps synchronous transmission from reducing the asynchronous bandwidth. Once synchronous transmission is done, the priorities of the asynchronous queues are evaluated and the frames from the highest priority queue are transmitted. The FORMAC Plus re-evaluates the decision to transmit each time a frame transmission is completed. If there are frames queued for transmission the FORMAC Plus checks the token-holding criteria to determine whether another frame can be sent (see FDDI specifications). The FORMAC Plus transmitter enters the transmit-idle state when reset.

SEND-IMMEDIATE MODE. When the FORMAC Plus is put into this mode using the NP instructions, it can transmit frames from the synchronous queue without capturing a token. This mode of operation can violate normal FDDI network operation and must be used with caution. In this mode FORMAC Plus does not perform any actions as a result of frames received on the RA or RB bus, including MAC frames; i.e., FORMAC Plus can't perform claim or beacon functions due to receive activity.

As soon as the FORMAC Plus enters the send-immediate mode, it loads the TRT with TMAX and, on expiration of TRT, it exits send-immediate mode and performs recovery if the late count was not zero. This provides an upper time bound for using send-immediate mode.

The following sequence of operations is needed to transmit frames using send-immediate mode:

(1) Reset the transmit queues.

(2) Load the frames to be transmitted into the synchronous queue.

(3) Give the command 'Enter Send Immediate Mode'.

(4) Unlock the synchronous queue.

In tag mode as soon as the 'Enter Send Immediate Mode' command is given, frames are unloaded from the buffer memory synchronous queue for transmission in the same way as is done in the normal mode for transmission from the synchronous queue except that FORMAC Plus will not use the TSYNC timer for ending transmission. Transmission is performed as long as FORMAC Plus is in send-immediate mode and frames are ready in the buffer memory synchronous queue for transmission.

In the nontag mode, after the FORMAC Plus is put into send-immediate mode, frames from the synchronous queue are transferred out of buffer memory for transmission as soon as the 'transmit synchronous queue' command is given. As long as FORMAC Plus is in this mode, it transmits each time a transmit command is given.

FORMAC Plus exits to the normal mode of operation when it receives the 'exit send immediate mode' command from NP, or when TRT expires. Send-immediate mode is state T6 in the state machine register.

Frame Transmission

If the FORMAC Plus has transmission requests pending, the next appropriate token (based on restricted/nonrestricted token mode) is captured. The requests are prioritized and data from the selected queue is loaded into the FORMAC Plus transmit FIFO. The FORMAC Plus will hold transmission of data if required to insure that at least 8 bytes (16 idle symbols) of preamble have been transmitted.

FORMAC Plus starts transmission by sending a start-delimiter (SD) on the X-bus immediately prior to transmission of the first frame byte from buffer memory. The frame check sequence (FCS) is appended after the last byte of the frame. FCS is not appended if the NFCS (no frame check sequence) bit in the frame's transmit descriptor word (in buffer memory) is set. After the FCS field, a 'T' and 'R' symbol are output on the upper and lower nibbles of the X-bus, respectively. These are the frame's end delimiter and error-status (E) indicators. This is followed by two more R's for the address (A) and copy (C) indicators in the upper and lower nibbles, respectively, in the last byte of the frame.

A transmit abort occurs in any of the following cases:

a. When the XMTABT (transmit abort) bit is set in the descriptor of the frame.

b. The frame underruns i.e., WPX = RPX.

c. The transmitter is forced into another state.

d. The command 'Abort Current Transmit' is issued using command register 2. In this case, the next byte to be placed on the X-bus is replaced by idles. The status transmit abort (SXMTABT) bit in status register 1 (bit 15 in ST1U) is set, and a token is issued to the ring. Transmission can still take place from other queues if transmission conditions exist. If not, a token is issued.

In the nontag mode, the start of a frame may be on any byte boundary in buffer memory. Two bits in the first byte of the frame descriptor are used to determine the byte boundary. These are theTXFBB1-0 (transmit frame byte boundary) bits. In essence, these bits act as two least significant bit extensions of the transmit read pointers to allow byte-boundary addressing. TXFBB1-0 can be different for each frame, if necessary.

Recovery Operation

The FORMAC Plus transmitter can go into recovery based upon frames received, instructions from the node processor, and timer expirations. There are two states in the FDDI transmitter state machine which are relevant to ring recovery operation. These are the claim and beacon states. Claim is used to negotiate the operative time for token rotation and determine which station will issue the token. Beacon is used to guarantee ring integrity by verifying the path of the ring.

Claim and beacon state can be entered at any time. Once claim or beacon state is entered, FORMAC Plus responds by placing the corresponding claim or beacon frames on the X-bus. The read pointer for transmitting special frames (RPXSF) is loaded with the contents of SACL or SABC and the claim/beacon frame is queued for transmission. In non-tag mode, using MORE bit in the frame descriptor, claim/beacon frames can be continuously sent. In tag mode, the frame is repeatedly sent until the FORMAC Plus is forced out of the claim/beacon state by virtue of receive state-machine transitions, or by issuing commands through command register 1.

Claim or beacon state can be entered during the transmission of a frame. In this case, the current transmission is aborted, the current transmit queue read pointer is updated to the next frame, and the transmit-abort-due-to-reset-or-recovery status bits are set in status register 1 (ST1U). FORMAC Plus can go from claim to beacon or beacon to claim. Each of these transitions sets the claim or beacon status bits in ST2U.

(4) On-Line-Special Mode

This operational mode is identical to the On-Line mode except that the 'A' and 'C' indicators (in the FS field) are not set on an external destination-address match and copy. This mode may be useful in bridge applications.

(5) Loopback Mode

Loopback mode is useful for 'in-circuit' testing of the FORMAC Plus and associated station hardware before insertion on the ring. Loopback operation can be performed in two modes: internal loopback and external loopback. If internal loopback is selected, the FORMAC Plus's X-bus is connected internally to the RA or RB bus input. Data on the RA and RB busses is ignored. If external loopback is selected, the loopback connection is assumed to be outside of the chip boundary.

When the FORMAC Plus is programmed for either of the loopback modes, the first four bytes following the frame source-address field are stored in the two MAC information registers (MIR). These two registers can be read from the NP bus. In full-duplex mode the FORMAC Plus also writes the entire received frame to the buffer memory if the conditions for receive exist. If the FORMAC Plus is programmed for half-duplex and is in transmit state, the received data is not written to buffer memory.

The internal timers are stopped during loopback mode. This prevents a timeout that could cause FORMAC Plus to unnecessarily enter the recovery state.

FORMAC Plus contains separate transmit and receive FCS generators. This allows FCS checking of received loopback frames while simultaneously transmitting in loopback.

NODE-PROCESSOR-BUS OPERATION

GENERAL. The NP can run on either a synchronous clock or on an asynchronous clock with respect to the byte clock (BCLK). See Figures 2, 3, and 4 for the timings of these signals. The NPMODE pin (external pin D3) must be strapped high to select FORMAC Plus synchronous operation and strapped low to select FORMAC Plus asynchronous operation.

Synchronous Mode

There are two possible methods for synchronous operation of the FORMAC Plus:

1. BMCLK frequency equals BCLK frequency (i.e. 12.5 MHz), and both clocks must be in-phase.
2. BMCLK operates at twice BCLK (i.e. BMCLK = 25 MHz), and both clocks must be in-phase.

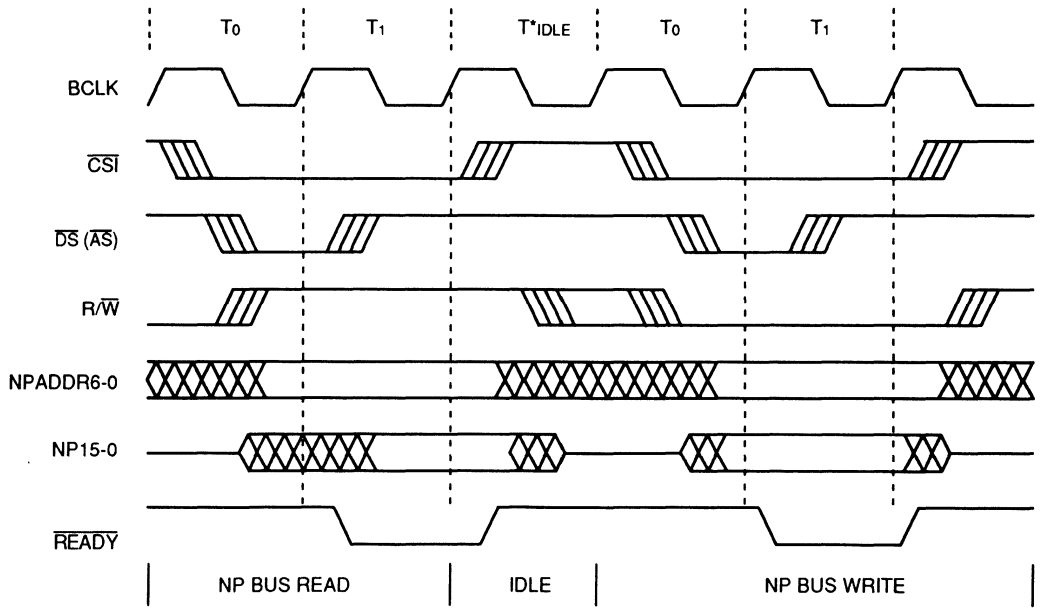
In either method, the $\overline{DS}$ (data strobe) should be active for only one BCLK cycle. All register accesses complete in two clock cycles and $\overline{READY}$ is asserted at the beginning of the second clock cycle. An exception is for MDR accesses that may take more than two clock cycles, at which point the assertion of $\overline{READY}$ is deferred until the last clock period of the execution cycle. $\overline{CSI}$ (chip select input) must go high (inactive) for at least one BCLK period between successive accesses.

Regardless of how many clock cycles are needed for executing an instruction, $\overline{READY}$ stays active only for one clock cycle.

Asynchronous Mode

In this mode, handshaking between the NP and the FORMAC Plus is used to indicate the completion of data transfer and instruction execution.

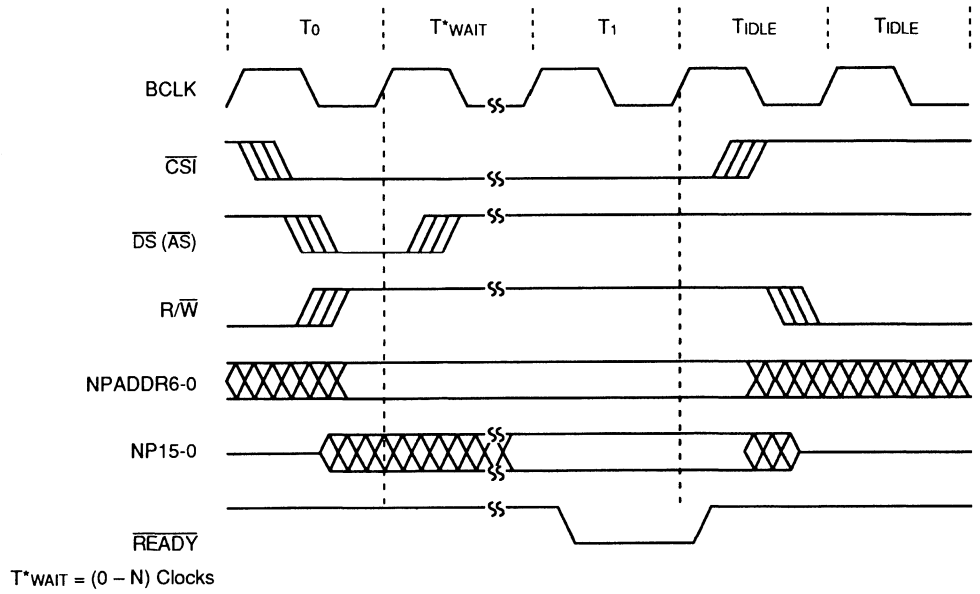
NP asserts the $\overline{DS}$ and $\overline{CSI}$ lines and issues an instruction on the NPADDR6-0 bus. FORMAC Plus synchronizes $\overline{CSI}$ and $\overline{DS}$ signals internally and then decodes the instruction. For a load instruction, FORMAC Plus latches the data into the internal register and then asserts $\overline{READY}$. For a read instruction, FORMAC Plus drives valid data on the bus and then asserts the $\overline{READY}$ signal. The $\overline{READY}$ signal stays asserted as long as $\overline{CSI}$ and $\overline{DS}$ both are active. Any one of them going inactive causes $\overline{READY}$ to go inactive.



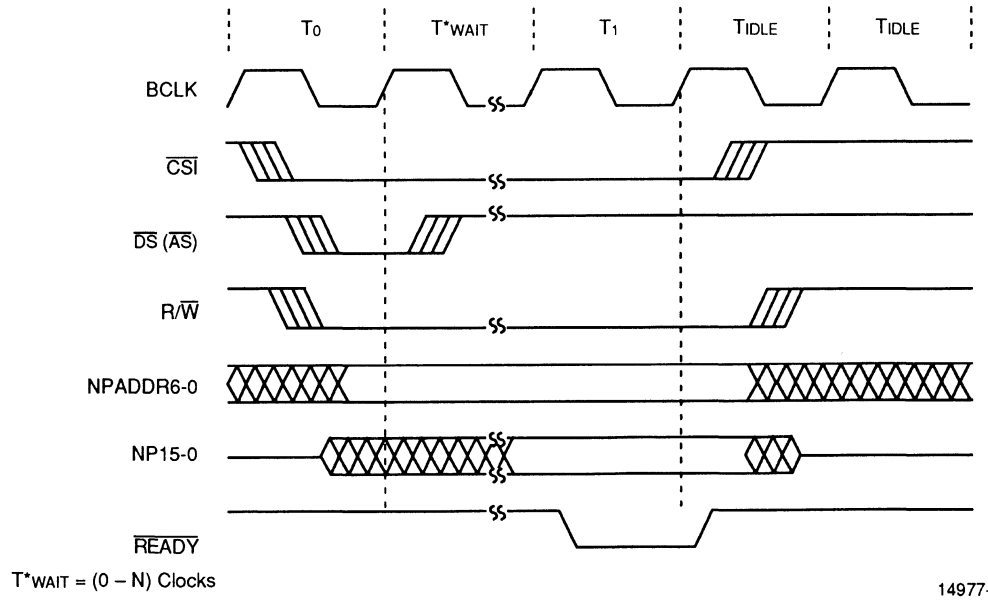
T^*_{IDLE} = (0 – N) Clocks

14977-005A

Figure 2. NP Bus Synchronous Read/Write Cycles

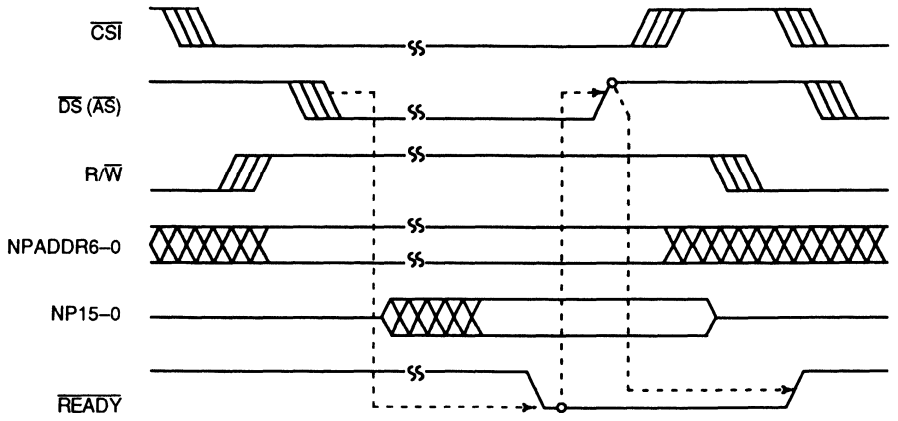


NP-Bus Synchronous MDRU/MDRL Read Cycle

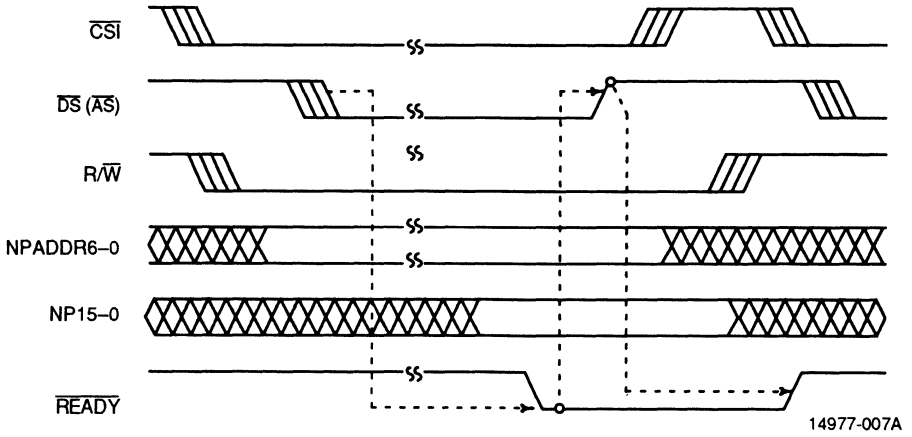


NP-Bus Synchronous MDRU/MDRL Write Cycle

Figure 3. NP-Bus Synchronous MDRU/MDRL Read/Write Cycles



NP-Bus Asynchronous Read Cycle



NP-Bus Asynchronous Write Cycle

Figure 4. NP-Bus Asynchronous Read/Write Cycles

BUFFER-MEMORY OPERATION

Introduction

GENERAL. Buffer memory management is performed in two distinct and independent ways depending upon the selection of the tag mode or nontag mode (see Figure 5). In tag mode FORMAC Plus provides local buffer management that is transparent to the host. Nontag mode is used when functional emulation of the previous-generation RBC/DPC/FORMAC local-buffer linked-list structure is desired.

LOADING END-ADDRESSES. Prior to any operation involving buffer memory, the NP must load the end addresses of all the queues. For the tag mode, the queue pointers should be in the order shown in Figure 5, i.e. in the order: special frame area, receive queue, synchronous queue, asynchronous queue 0, asynchronous queue 1, and asynchronous queue 2. For the non-tag mode, only EACB and EARV need to be in the order shown in Figure 5 and other transmit queues (synchronous, asynchronous 0, ansynchronous 1, and asynchronous 2) may be organized in any order. If any queue is to be ignored, its end address must be the same as that of the previous queue. For example, if the synchronous queue is to be ignored, then the pointer EAS = EARV. The NP must also program the read/write pointers of all the queues being used. After the FORMAC Plus has been initialized, the memory-active mode may be entered to allow the loading of special frames into the special-frame area. Special frames are: claim, beacon and auto-void frames. During the memory-active mode the FORMAC Plus neither receives frames nor responds to claim or beacon conditions. After the special frame is loaded into memory, the on-line mode may be entered for normal operation.

In tag mode the pointers associated with the claim/beacon frames can be changed while FORMAC Plus is in any mode, whereas, to insure correct operation, all the other pointers should be changed only when FORMAC Plus is in the initialize mode.

In the nontag mode the claim/beacon (SACL/SABC) pointers can be changed in any mode. However, it should be noted that the RPXSF register is loaded with the changed pointer only when FORMAC Plus next enters claim/beacon state.

USE OF LSB BIT. In the nontag mode, the FORMAC Plus provides two ways of organizing the bytes within long words in memory: When the LSB bit in MDREG2 is set (high), the least significant byte in a long word is transmitted/received first. When LSB is low, the most significant byte of a long word is transmitted/received first. The order of bits in a byte is not changed. The state of the LSB bit does not affect the byte ordering of the pointer/descriptor/status words.

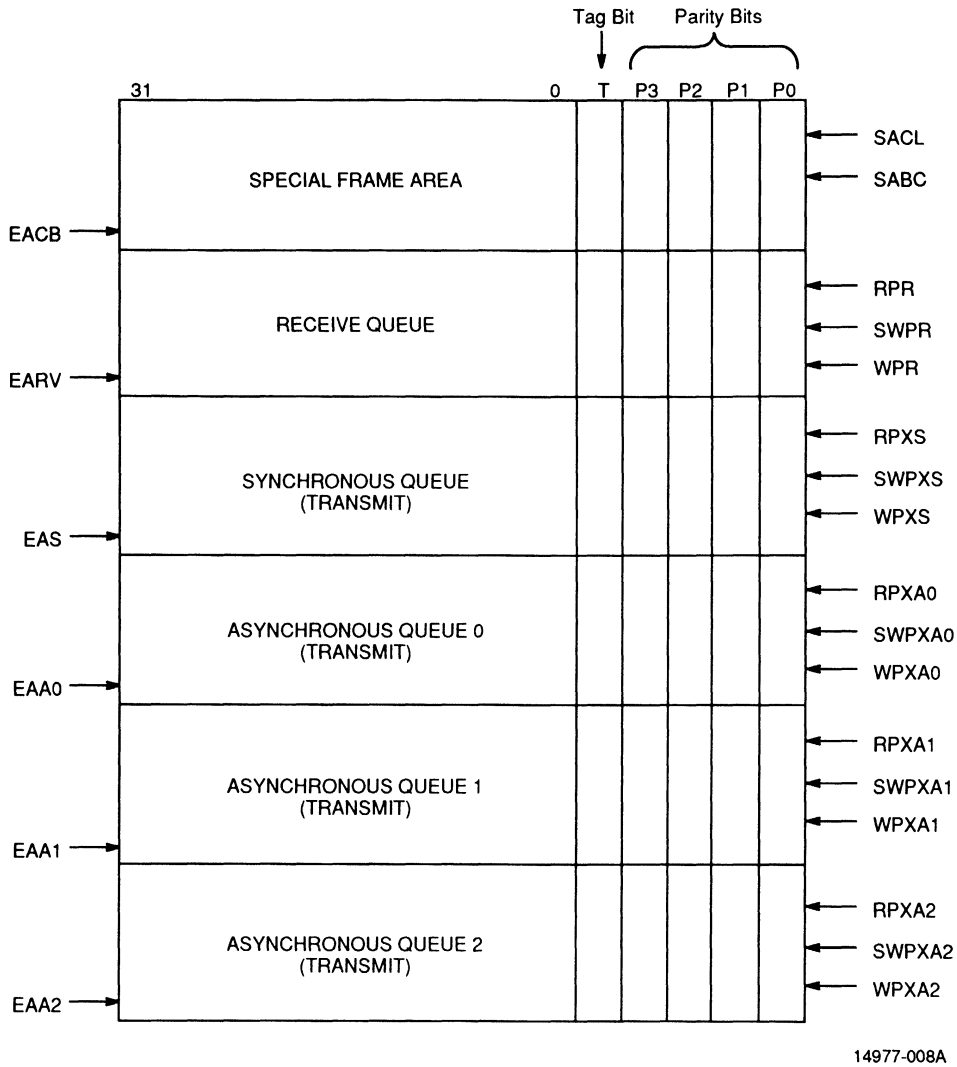


Figure 5. Buffer Memory Organization (Tag Mode and Nontag Mode)

Tag Mode

Loading of Transmit Frames (tag mode)

TRANSMIT-FRAME FORMAT. Transmit frames (See Figure 6) in the tag mode must consist of aligned data, i.e. all words in buffer memory must contain four valid bytes, except that the last data word may consist of less than four bytes. The frame data is always followed by a descriptor word. The last data word (or partial word) in the frame, and the descriptor word, have their tag bits set to 1.

Upon host request, transmit frames are loaded from the host into the buffer memory under control of the FORMAC Plus. Requests are serviced based on the state of the queue being requested. FORMAC Plus acknowledges each request in one of the following ways:

1. If the requested transmit queue has space for more frames, then FORMAC Plus acknowledges the request and the three QCTRL pins are output as all 0's.
2. If the number of free long words in the requested transmit queue is exactly two times the value of AFULL3-0 (in mode register 2), FORMAC Plus acknowledges the request and QCTRL indicates the 'almost full' condition.
3. If the requested transmit queue is full, FORMAC Plus does not acknowledge the request, the three QCTRL

pins are all 0's, and the status transmit buffer full bit (STBFLS or STBFLA (in ST1U)) for that queue is set.

4. If the requested transmit queue has underrun and the host has placed a write request for this queue, then the QCTRL pins indicate the "abort this transmit frame" (underrun) condition.
5. If the full or underrun condition has not occured for the requested transmit queue, FORMAC Plus acknowledges the request and the write pointer for the requested queue (WPXS or WPXA0-2) is incremented. If the word written into the buffer memory has the tag bit set to 1, indicating the last data word of the frame, the next word (the descriptor) must also have the tag bit set to 1. When the descriptor is written, the shadow-write pointer for the requested queue (SWPXS or SWPXA0-2) is loaded with the value of the write pointer of the requested queue (WPXS or WPXA0-2), which points to the beginning of the next frame.

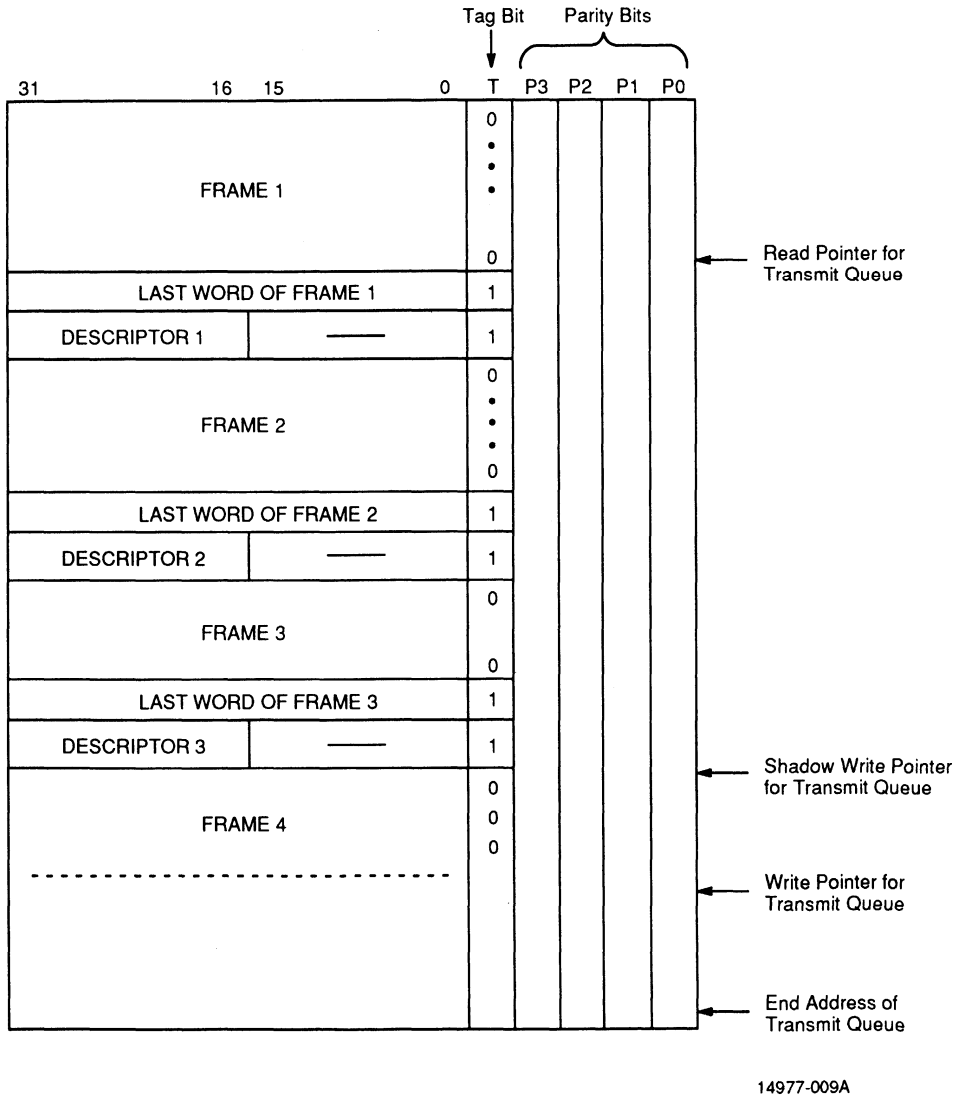


Figure 6. Buffer Memory Transmit Queue (Tag Mode)

Frame Transmission From Buffer Memory (tag mode)

TRANSMISSION CRITERIA. A frame is ready for transmission when either of the two following conditions is satisfied:

1. The buffer-memory tag-bit signal BDTAG equals 1. This means that the last-word and descriptor-word tag-bits of a frame both equal 1, thus indicating that the frame has been completely loaded into buffer memory.
2. The number of long words currently in buffer memory exceeds the transmit-frame threshold value XTHR (in the FRMTHR register) and the value in XTHR is not equal to zero.

TRANSMISSION OF QUEUES. When a token is captured, transmission of a queue can begin. If all of the following three conditions are satisfied, frames are read in from buffer memory for transmission by FORMAC Plus until a tag bit set to 1 is encountered:

1. FORMAC Plus is not in send-immediate mode.
2. TRT and TMSYNC have not expired, if synchronous frames are present and transmission criteria (above) are met.
3. Both TRT and THT have not expired, if asynchronous frames are present and transmission criteria (above) are met.

END OF QUEUE. As long as transmission conditions are satisfied, frames are read in for transmission until the read pointer value for the queue being transmitted (RPXS or RPXA0-2) is equal to the shadow write pointer value for this queue (SWPXS or SWPXA0-2).

While transmission is in progress, and after complete transmission of a frame, FORMAC Plus fetches more data from this queue into its on-chip transmit FIFO for transmission only if the write pointer value, WPXx minus the shadow write-pointer value SWPXx (where x = S, A0, A1 or A2 for the queue), exceeds the threshold (XTHR) programmed in the frame-threshold register. FORMAC Plus checks queues for transmission until the token is released.

Transmission from a queue is completed when RPXx = WPXx, or RPXx = SWPXx, and WPXx – RPXx < XTHR (where x = S, A0, A1 or A2 for the queue).

If the read pointer for the queue being transmitted (RPXS or RPXA0-2) becomes equal to the write pointer for that queue (WPXS or WPXA0-2), and the transmit FIFO empties in the middle of a frame, an underrun condition is implied. If this condition is encountered, the current frame is aborted and the appropriate bit in the lower half of status register 1 (ST1L, bits 12–15), i.e. STBURS or STBURA0-2, is set. If the host tries to load the queue, FORMAC Plus does not acknowledge the request and the QCTRL bits indicate 'abort this transmit frame'. When this QCTRL message is encountered, the host aborts transfers of the rest of the frame to buffer memory.

Transmitting Send-Immediate Frames from Buffer Memory (tag mode)

In send-immediate mode transmission of frames is done from the synchronous queue exactly as in normal operation, except that FORMAC Plus does not wait for a token in order to transmit frames.

Loading of Claim/Beacon/Auto-Void Frames (tag mode)

Claim/beacon/auto-void frames (also called special frames) reside in the buffer-memory special-frames area (see Figure 5). The format of these special frames must be the same as that of the transmit frames, and the last word and descriptor word must have their tag bits set to 1.

There can be several claim and beacon frames but only one auto-void frame (starting at location 0000) in the special frames area. The special frames are loaded one at a time. The NP loads the WPXSF (write pointer transmit special frames) with the appropriate address of the frame and then instructs the host to load the special frame.

The special frames are loaded by the host into buffer memory under the control of FORMAC Plus. The host makes an encoded request on the HSREQ2-0 pins to FORMAC Plus to load the special frame. FORMAC Plus acknowledges the request. Special frames must be completely loaded before transmission begins. When the NPMEMRQ pin is used by the NP (or DMA), the address bus and memory control signal lines are placed in the high-impedance state by the FORMAC Plus. This gives the NP (or DMA) free access to load buffer memory (the frames must conform to the format defined).

When the NP uses the MARW and MDR to load buffer memory, it first loads the MARW with the starting address of the frame. Then the MDRU (memory data register upper 16-bits) is loaded from the NP-bus followed by the MDRL (memory data register lower 16-bits). As soon as the second 16-bit data word is loaded, FORMAC Plus sets an internal request to move the contents of the MDR to the buffer memory. The MARW is incremented after the write operation is completed. Any new request to load the MDR is held (i.e., $\overline{\text{READY}}$ not asserted) until the previous transfer to memory has been completed. The last word and descriptor word must have their tag bit set to 1. To do this, use the command-register-2 Set Tag Bit command.

Note: At least one claim and one beacon frame must be loaded in the special-frame area before FORMAC Plus is set ON-LINE. To change a claim/beacon frame while FORMAC Plus is ON-LINE, the user must load the new claim/beacon frame at a free location in the special frames area and then change the SACL or SABC (start address claim/beacon) pointers.

The auto-void frame must be loaded at location 0000 before FORMAC Plus enters the restricted-token mode. When in restricted-token mode, a single auto-void frame is automatically transmitted after the reception of a restricted token if there are no frames queued for transmission. Transmitting an auto-void frame ensures that stations in nonrestricted token mode will have their TVX timers reset during restricted dialogues. Auto-void frames have a destination address of all zeros.

Transmitting Claim/Beacon/Auto-Void Frames (tag mode)

Of the several claim and beacon frames that may be stored in the special frames area, the addresses of the selected claim frame and beacon frame are stored in the address registers SACL (start address claim) and SABC (start address beacon) respectively.

When a claim/beacon frame is to be transmitted, the FORMAC Plus loads RPXSF (read pointer transmit special frame) with the contents of SACL/SABC and reads the claim/beacon frame for transmission. At the end of a transmission, the RPXSF is reloaded from the SACL/SABC and the cycle repeats until the FORMAC Plus is forced out of the claim/beacon state.

When a void frame needs to be sent out, the RPXSF is loaded with 0000 and the frame is read out for transmission. Hence, before FORMAC Plus enters the restricted-token mode, the void frame should be stored at the location 0000. The status conditions of the special frames are reflected by the status SERRSF bit in ST2U (bit 7).

Loading Receive Frames into Buffer Memory (tag mode)

In a receive frame (tag mode), a 16-bit status word and a 16-bit frame-length word make up the last long word of the frame. Also, the tag-bit of this last long word is set to 1. See Figure 7.

When the receive buffer queue has an overflow condition during frame reception, the status register bit indicating an overflow error in the receive queue, SRBFL (in ST2U, bit 12), is set high. When the FORMAC Plus encounters a buffer-full condition, it stops writing data into the buffer memory. If the frame is an aborted frame, then its status word contains the receive-abort condition.

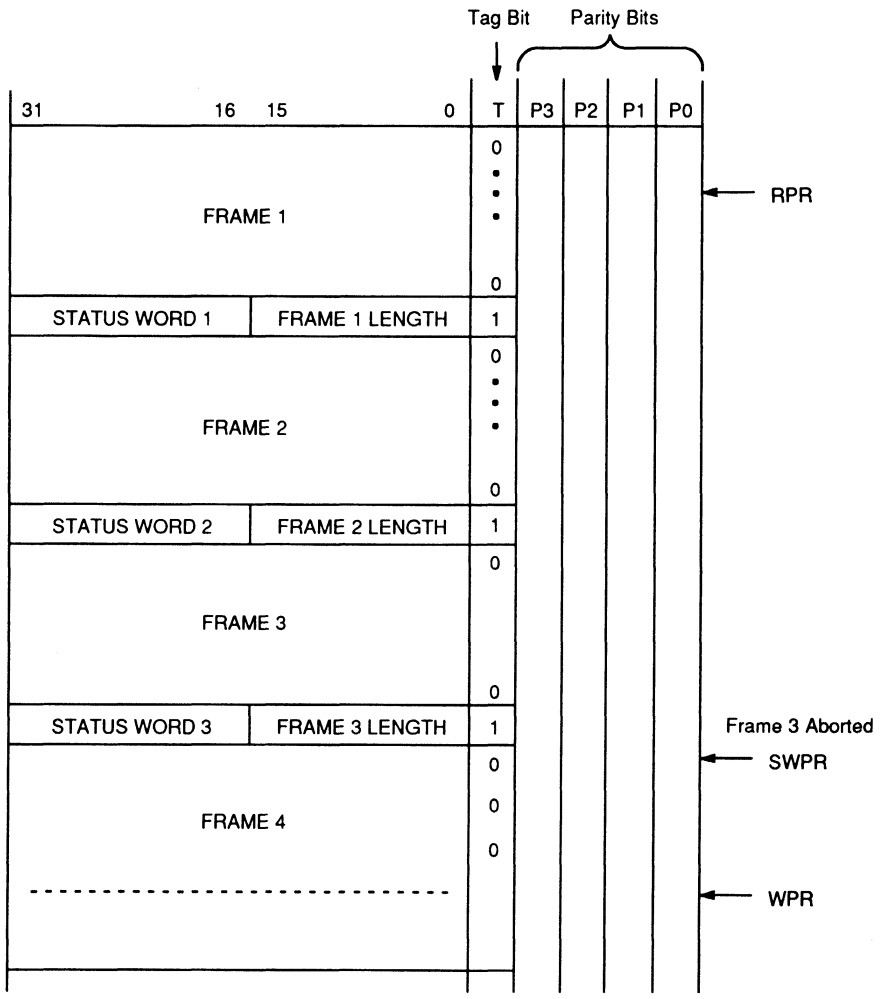
The receive frames are loaded into the buffer memory by FORMAC Plus, which can be programmed (in MDREG1) for single-frame receive mode (SNGLFRM = 1) or multi-frame receive mode (SNGLFRM = 0). The RDATA timing depends upon the receive threshold value programmed into the frame threshold register in multi-frame receive mode.

LOADING IN MULTI-FRAME RECEIVE MODE (tag mode). RDATA is set high either when the number of long words in the buffer memory exceeds RTHR times 4 if RTHR is not equal to zero, or when a complete frame is received in buffer memory.

After the frame (data) has been written into buffer memory, FORMAC Plus writes the status word and the length of the received frame (tag-bit = 1 indicating the end of the frame) in bytes at the end of the frame just received. RDATA remains high until all the completed frames in the receive queue (in buffer memory) have been read out by the host.

LOADING IN SINGLE-FRAME RECEIVE MODE (tag mode). In this mode FORMAC Plus interrupts the NP by setting the SRCVFRM (receive single frame) bit in status register 2 (ST2U) when either of the following occurs:

1) The number of received-frame long words written into buffer memory exceeds RTHR times 4 if RTHR is not equal to zero.
2) The status word is written in the buffer memory for a frame.



Note:

In this example, frame 3 was aborted due to error conditions (i.e., RCVABT = 1)

Figure 7. Buffer Memory Receive Queue (Tag Mode)

Unloading Receive Frames from Buffer Memory (tag mode)

The RDATA line enables the host to unload the receive frame. If the host makes a read request while RDATA is high, the FORMAC Plus acknowledges the request.

UNLOADING IN MULTI-FRAME RECEIVE MODE (tag mode). When the RPR pointer reaches the end of a frame, if the receive queue in buffer memory is empty or the receive queue contains only a partial frame that has not crossed the receive threshold, the RDATA signal goes low.

UNLOADING IN SINGLE-FRAME RECEIVE MODE (tag mode). When FORMAC Plus interrupts the NP using SRCVFRM bit in status register 2 (ST2U), it expects NP to give an 'enable single frame receive' command. When FORMAC Plus decodes this command it asserts the RDATA signal high for transfering the received frames out of buffer memory. The RDATA signal is deasserted (low) when the following two conditions are valid:

1. When the RPR pointer reaches the end of a frame (tag bit = 1).
2. When any of the following three conditions is satisfied:
   a) The receive queue contains only a partial frame that has not crossed the receive threshold.
   b) The receive frame counter is zero.
   c) No new 'enable single frame receive' is received from the NP.

Nontag Mode

Loading Transmit Frames (nontag mode)

GENERAL. The format of a transmit frame (Figure 8) in the nontag mode consists of a descriptor word, followed by data words, followed by a pointer word. This format is the same as that supported by the prior-generation RBC/DPC/FORMAC chips. The descriptor word includes the length of the frame in bytes. The pointer word contains the address of the descriptor for the following frame. The first and last data words can be partial words (less than 4 bytes). The location of the first byte in the first long word is defined by the byte-boundary bits in the descriptor word. For formats of the pointer and descriptor see the discussion under Data Handling and Formats.

Transmit frames are loaded by the host into the buffer memory either by using the host request pins, or by NP (or DMA) transfers using the NP memory request pin, or by using the FORMAC Plus registers: MARW (memory address register for writes) and MDR (memory data register).

When using the host request pins, FORMAC Plus responds to the host requests as in the tag mode (see loading of transmit frames) except that the QCTRL signals will be always '0'. FORMAC Plus does not monitor the frames being loaded into buffer memory for memory-full conditions, etc.

When the NPMEMRQ pin is used by the NP (or DMA), the address bus and memory control signal lines are placed in the high-impedance state by the FORMAC Plus. This gives the NP (or DMA) free access to load the buffer memory (the frames must conform to the format defined).

When the NP uses the MARW and MDR to load buffer memory, it first loads the MARW with the starting address of the frame. Then the MDRU (memory data register upper 16-bits) is loaded from the NP-bus followed by the MDRL (memory data register lower 16-bits). As soon as the second 16-bit data word is loaded, FORMAC Plus sets an internal request to move the contents of the MDR to the buffer memory. The MARW is incremented after the write operation is completed. Any new request to load the MDR is held (i.e., $\overline{\text{READY}}$ not asserted) until the previous transfer to memory has been completed.

Chained Transmit Operation (nontag mode)

A group of frames constitutes a chain (Figure 9). The MORE bit (bit 31) in a frame descriptor, when 0, denotes the last frame in a chain. The entire chain can be queued for transmission by issuing a transmit instruction. FORMAC Plus transmits the entire chain and stops after the frame in which the MORE bit equals 0. FORMAC Plus assumes that no frame, descriptor, or pointer associated with the frames in the chain will be modified once the transmit instruction is issued. Additional frames for transmission (after the transmit instruction) have to be queued in a second chain and a new transmit instruction issued. FORMAC Plus can pipeline and remember two transmit instructions per transmission queue, i.e., two chains (of the same transmit queue) can be queued at any time.

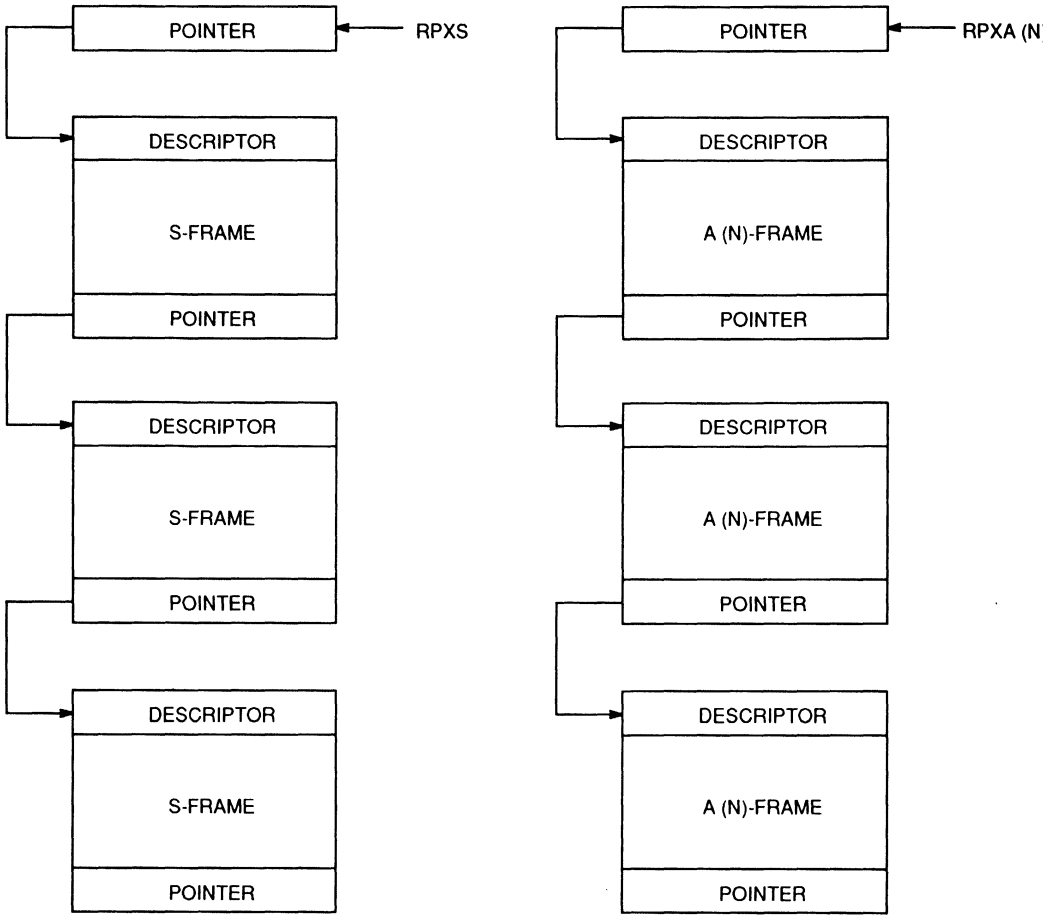


Figure 8. Buffer Memory Transmit Queues (Nontag Mode)

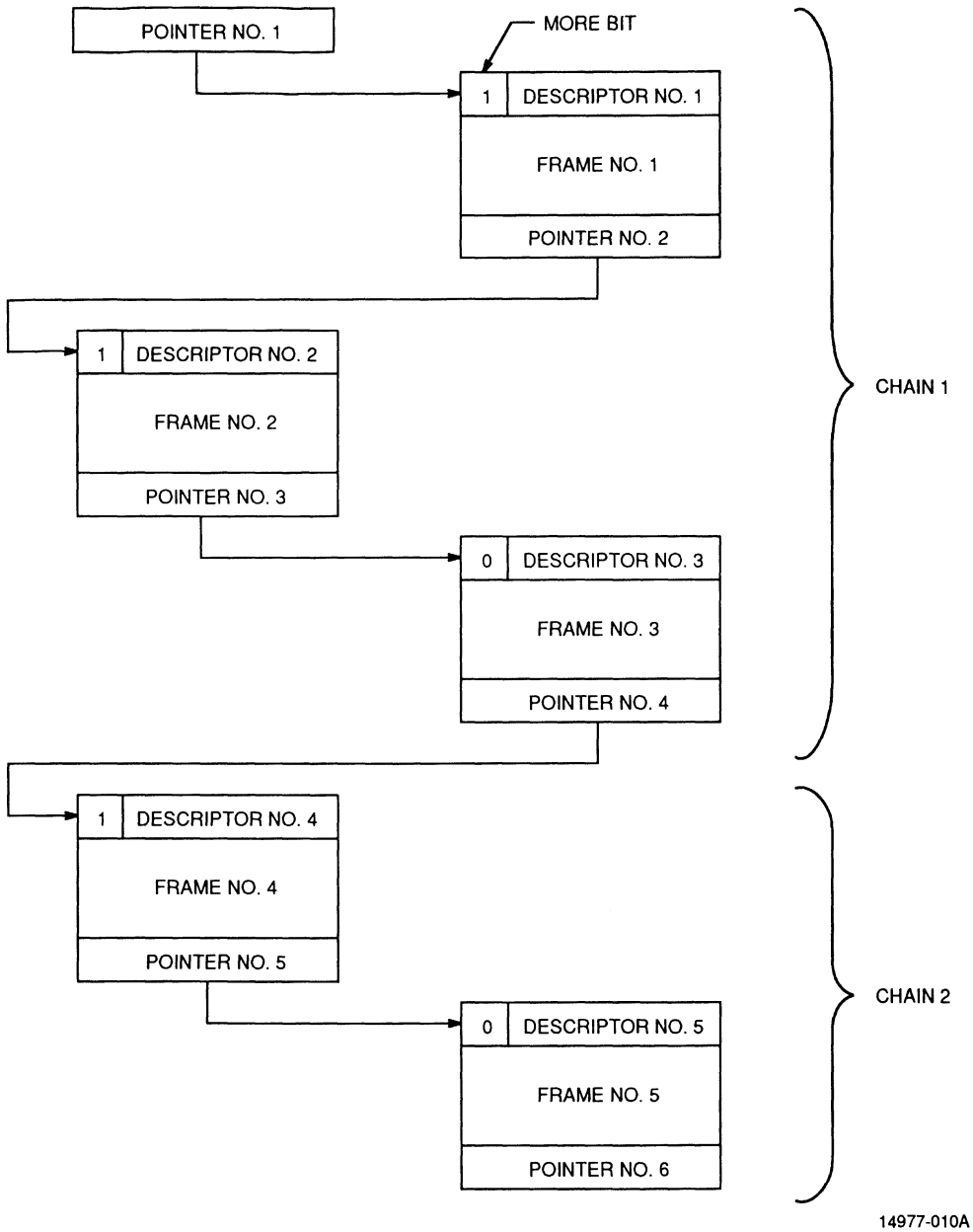


Figure 9. Buffer Memory Transmit Chains (Nontag Mode)

Transmission of Transmit Frames (nontag mode)

After the complete frame(s) have been loaded for transmission, the NP gives an instruction to FORMAC Plus to transmit the appropriate queue(s). After the transmit instruction has been issued, a token is captured if the transmission conditions have been satisfied (i.e. the TRT for synchronous frames, and TRT or THT for asynchronous frames, must not have expired), and the frame is read in by the FORMAC Plus. The first long word read is the pointer of the previous frame, followed by the descriptor word of the new frame to get the length of the frame. Then the rest of the frame is read, using the length information. If the descriptor has the MORE bit (bit 31) set, FORMAC Plus moves to the next frame.

FORMAC Plus can have two chains queued in each of the transmission queues, i.e. the NP can issue a second instruction for transmission while the first instruction is queued or being serviced. At the end of the first chain when the MORE bit is 0, if a second chain has been queued-up and a second transmit instruction has been issued, FORMAC Plus treats this as a continuation (as if the MORE bit was '1'), or else FORMAC Plus quits transmitting the current queue. If the XDONE bit is set, then FORMAC Plus quits transmitting the current queue until the next token is captured.

Loading Claim/Beacon/Auto-Void Frames (nontag mode)

The format of the claim/beacon/auto-void frames (i.e. special frames) is the same as for transmit frames.

There can be several claim/beacon frames but only one auto-void frame. These special frames can be loaded into the buffer memory either by using the WPXSF (Write Pointer Special Frame) instruction through the node processor and the host interface, or by the NP only. In the first case, the NP loads the WPXSF with the appropriate address of the frame and then instructs the host to load the special frame. Special frames must be completely loaded before FORMAC Plus enters the ON-LINE mode.

RESTRICTED-TOKEN MODE. An auto-void frame must be loaded at location 0000 before FORMAC Plus enters the restricted-token mode. When in restricted-token mode, a single auto-void frame is automatically transmitted after the reception of a restricted token if there are no frames queued for transmission. Transmitting an auto-void frame ensures that stations in non-restricted token mode will have their TVX timers reset during restricted dialogues. Auto-void frames have a destination address of all zeros.

Claim/beacon/auto-void frames can also be loaded into buffer memory by using the MDR and the memory address register for random writes (MARW), or by using the NPMEMRQ pin (DMA).

Transmitting Claim/Beacon/Auto-Void Frames (nontag mode)

The FORMAC Plus address register SACL (start address Claim) must be programmed with the 16-bit Buffer Memory address of a 16-bit pointer which points to the Claim frame (see Figure 8).

The SABC (start address Beacon) register must be programmed in a similar manner with the 16-bit Buffer Memory address of a 16-bit pointer which points to the Beacon frame.

When a Claim/Beacon frame is to be transmitted (internal request) the FORMAC Plus loads RPXSF (read pointer transmit special frame) with the contents of SACL/SABC. The FORMAC Plus then loads RPXSF with the contents of the 16-bit pointer to the Claim/Beacon frame, then reads the Claim/Beacon frame for transmission.

For sending the same Claim/Beacon frames continuously, the MORE bit of the descriptor should be set and the pointer should point to the beginning of the same frame. If different Claim/Beacon frames are to be sent during the Claim/Beacon process, then new frames have to be stored in Buffer Memory and the SACL/SABC register has to be reprogrammed with the new address pointing to the 16-bit pointer pointing to the new frame.

The Auto-Void frame may be located anywhere in Buffer Memory. However, the 16-bit pointer to the Auto-Void frame is required to be loaded at location 0000 in Buffer Memory. When the Auto-Void frame needs to be transmitted, the FORMAC Plus automatically loads the RPXSF with the 16-bit pointer at location 0000, and then the Auto-Void frame is read out for transmission.

The status condition of the special frames is reflected by the SERRSF status bit (bit 7) in ST2U.

Send-Immediate Frames (nontag mode)

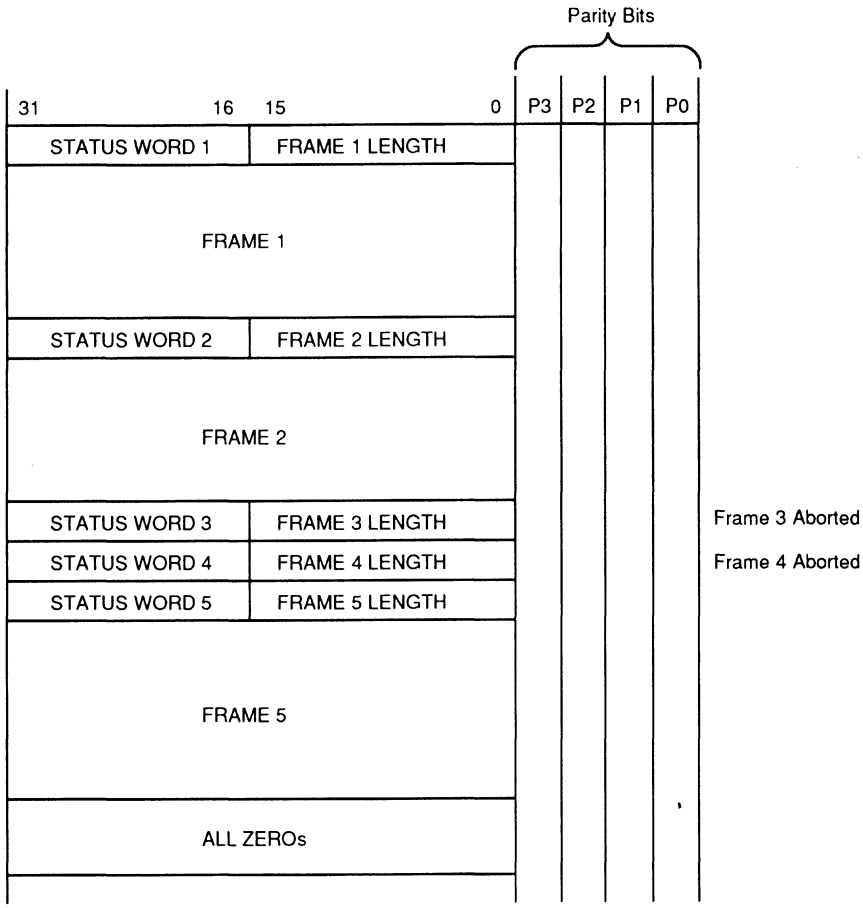
The frames for immediate transmission in send-immediate mode are transmitted from the synchronous transmit queue and obey all the same loading and unloading rules as in normal synchronous transmission except for TSYNC checking. However, in send-immediate mode FORMAC Plus does not wait for a token in order to transmit a frame.

Loading Receive Frames (nontag mode)

FORMAT OF RECEIVE FRAME. The format of a receive frame is shown in Figure 10. The first long word of each frame consists of a 16-bit status word and a 16-bit word that gives the length of the frame in bytes. See Figure 17 for a diagram of the receive-frame status/length word. The status/length word is followed by the data words. The location of the first byte in the first long word of data is defined by the byte boundary bits RXFBB1-0 of MDREG2 (mode register 2). At the end of the frames that make up a receive queue, FORMAC Plus writes a long word whose most significant bit (bit 31) is a logic 0, which indicates that there is no more data in this queue. The only function of this word is to act as an end delimiter. All its bits are filled with 0's. Note that the MSVALID bit in bit 31 of the status word at the start of the frame is always in the logic 1 state. Also, when another frame follows this queue, it overwrites the end-delimiter word with the receive-status word of the new frame.

After each frame has been written into buffer memory, FORMAC Plus writes the status and frame length at the start of each frame, and places an end-indicator word of

all 0's at the end of the queue. Once a frame is completely received, the status bit SRCOMP in status register 2 (ST2U) is set. If the receive queue has an overflow condition during frame reception, the status register bit indicating an overflow error in the receive queue, SRCVOVR in ST2U (bit 11), is set high and the frame is aborted. An overflow also sets the MSRABT bit (bit 30 in the receive-frame status word).



Notes:
In this example, frames 3 and 4 were aborted due to error conditions.
Bits 31–0 of last word in queue are all zeros.

Figure 10. Buffer Memory Receive Queue (Nontag Mode)

Unloading Receive Frames (nontag mode)

Received frames are unloaded by the host from the buffer memory by using the host request pins (HSREQ), or by using the NP memory request pin (NPMEMRQ), or by using the FORMAC Plus MARR and MDR registers.

When using the host-request pins (HSREQ), FORMAC Plus responds to host requests as in the tag mode. The RDATA and QCTRL signals are always in the 0 state. When the NPMEMRQ pin is used for NP DMA, the address bus and memory control signals are released by the FORMAC Plus. Here, the NP DMA process has full control in unloading buffer memory.

When the NP uses the MARR and MDR to read the buffer memory, it first loads the MARR with the starting address of the received frame. Then, either the read memory with address increment (IRMEMWI) or the read memory without address increment (IRMEMWO) instruction is issued by the NP to read the buffer memory location addressed by the MARR and transfer its contents to the MDR. The NP then reads the MDR (MDRU and MDRL). The read will not be acknowledged (i.e., $\overline{\text{READY}}$ not asserted) until the data is fetched from the buffer memory into MDRL and MDRU. For IRMEMWI, once an MDR read (i.e., read both MDRU and MDRL) is completed, FORMAC Plus loads the MDR with the contents of the next location in buffer memory. The MARR is incremented after every read.

INTERFACING WITH THE PHYSICAL LAYER (PHY)

The physical-layer/FORMAC Plus interface is synchronous to BCLK. There are two receive buses (RA and RB) coming into the FORMAC Plus. The SELRA bit in MDREG1 register selects the bus to be used as the active FORMAC Plus media input. The RA bus is selected if SELRA is 1; otherwise the RB bus is selected. SELRA is not affected by either hardware reset ($\overline{RST}$) or a reset command. A single transmit bus (X-bus) outputs to the physical layer. Note that when FORMAC Plus is in the on-line mode, the receive and transmit buses are always active.

STATUS AND INTERRUPTS

Introduction

Two 32-bit read-only registers, designated ST1 and ST2, are dedicated to status handling and interrupt reporting. Any of the bits in these status registers can be used to generate an interrupt. The bits in status register 1 (ST1) are routed to the $\overline{MINTR1}$ pin and the bits in ST2 are routed to the $\overline{MINTR2}$ pin. The bits in both ST1 (see Figures 11 and 12) and ST2 (see Figures 13 and 14) may be masked by the interrupt mask registers (IMSK1, IMSK2) for complete control of the interrupt conditions. Because the NP bus is 16 bits wide, each 32-bit status register is addressed in two halves, each of which has a separate address. For ST1 the halves are designated as ST1U and ST1L for the upper and lower 16 bits, respectively. Similarly, for ST2 the halves are addressed as ST2U and ST2L.

Remember the following points when responding to an interrupt from FORMAC Plus. This discussion applies to both interrupts.

1. After the user software senses a FORMAC Plus generated interrupt, both halves of the corresponding status register must be read before the interrupt line can again be asserted by FORMAC Plus. **Note:** The two halves of a status register each has a separate address, and can be read in any order.
2. After either half is read, FORMAC Plus deasserts and locks the interrupt line until the remaining half is read.
3. Reading the first half can be done any number of times before reading the second half. Reading the second half unlocks the interrupt and normal operation resumes.
4. Any new status-change conditions that affect the first half after it is read are not applied until after the second half is read. This also means that any new status-change conditions that affect the second half after the first half is read but before the second half is read are in fact applied to the second half and are included in its status when it is read.
5. Reading the second half removes the lock on the interrupt line, and it is then free to be asserted if any unmasked status bit is set.

Status Register 1 (ST1)

Status register ST1 contains the status bits that can generate maskable interrupts on the $\overline{MINTR1}$ pin. ST1 has status bits associated with transmit operations. All status bits except the queue-locked bits are auto-cleared on reading the register. The queue-locked status bits SQLCKx (where x = S, A0, A1, or A2) can be cleared only using instructions through command register 1.

Whenever any of the bits of status register 1 causes an interrupt on $\overline{MINTR1}$, the user must read all 32 bits of ST1 to enable any future interrupt generation.

A FORMAC Plus reset clears both the upper and lower 16 bits of the register except the bits SQLCK (S, A0, A1, A2) and STXINFL (S, A0, A1, A2). The following paragraphs describe the functions of the ST1 bits.

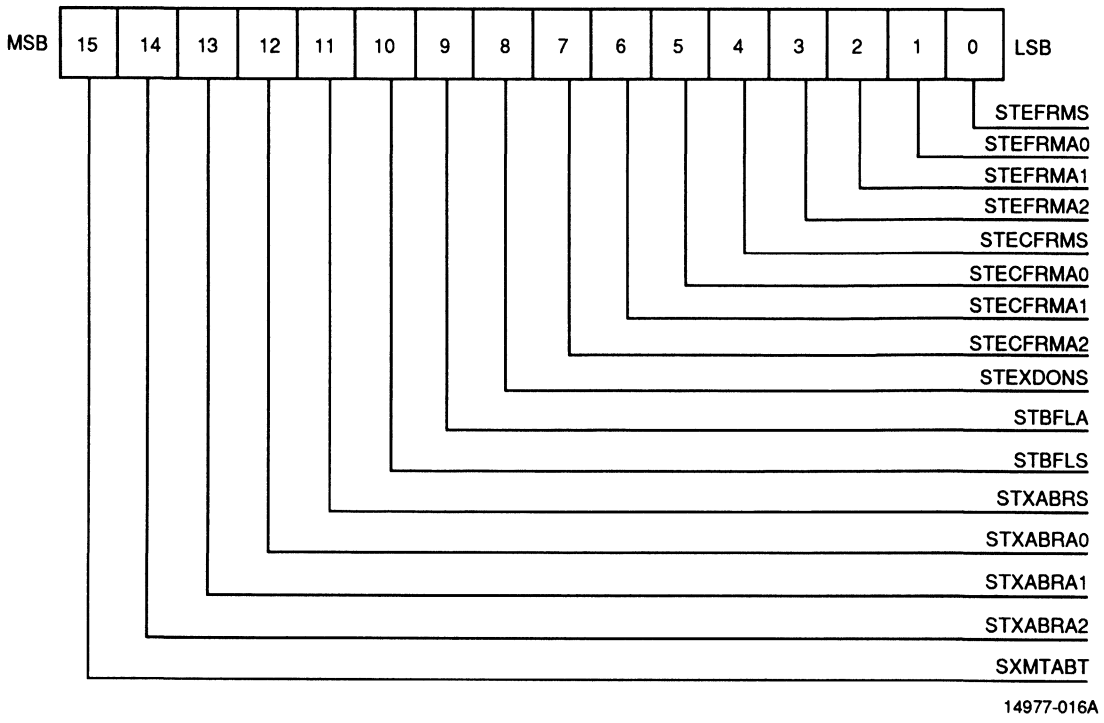


Figure 11. Status Register 1 – Upper 16 Bits (ST1U)

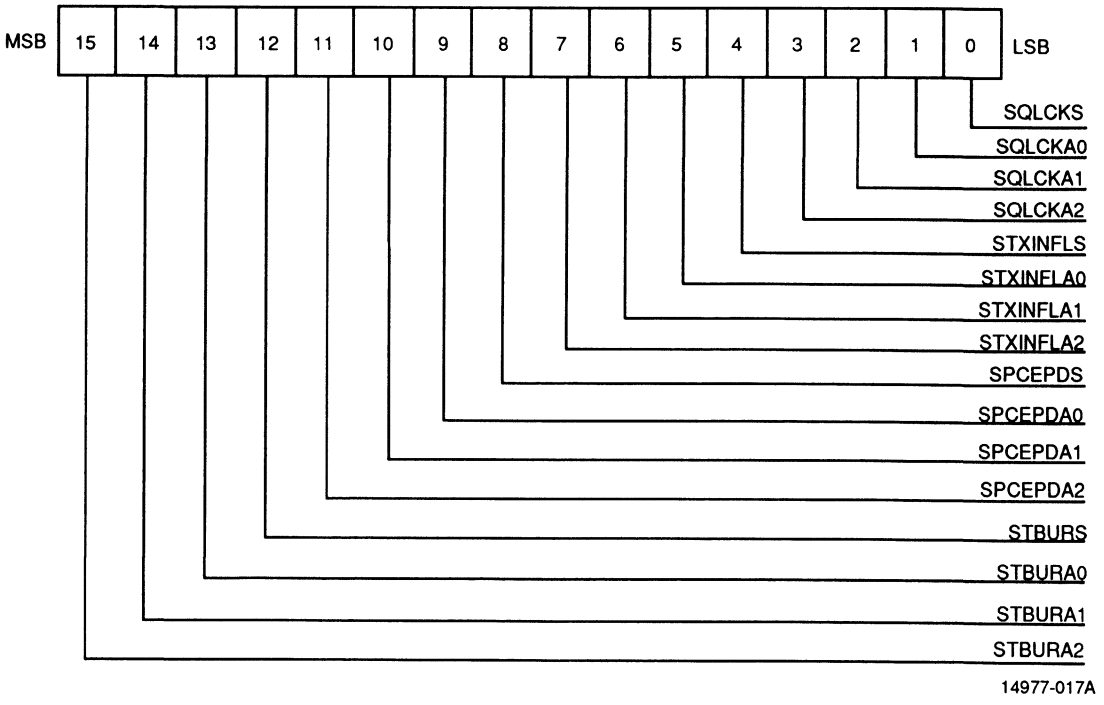


Figure 12. Status Register 1 – Lower 16 Bits (ST1L)

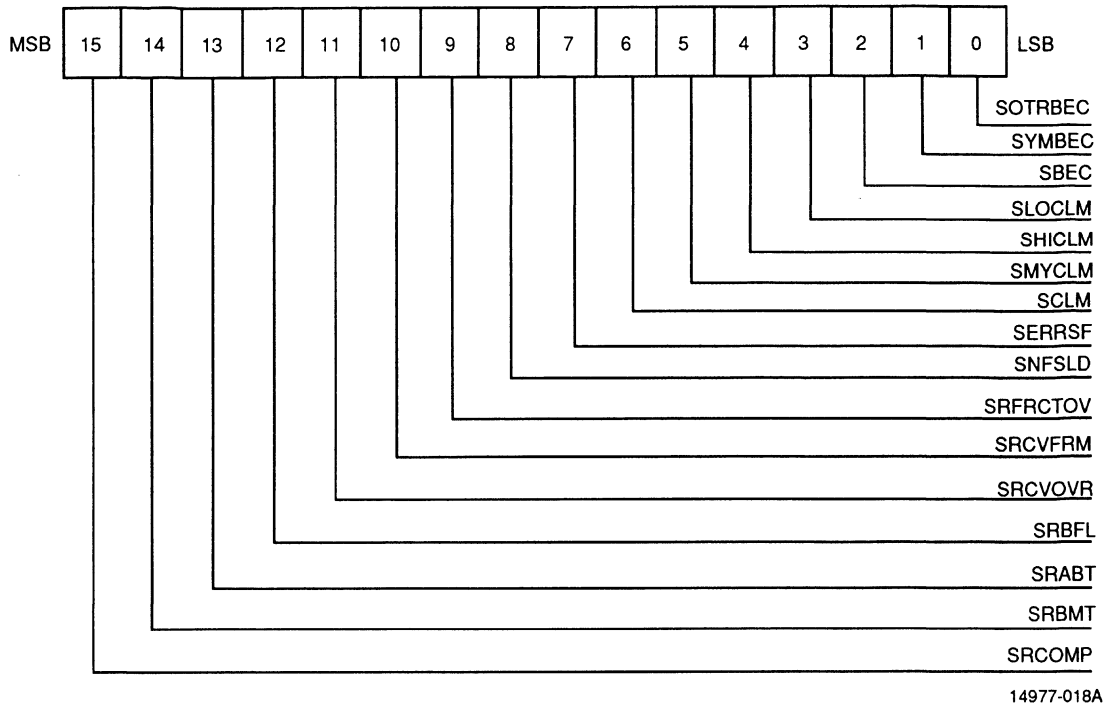


Figure 13. Status Register 2 – Upper 16 Bits (ST2U)

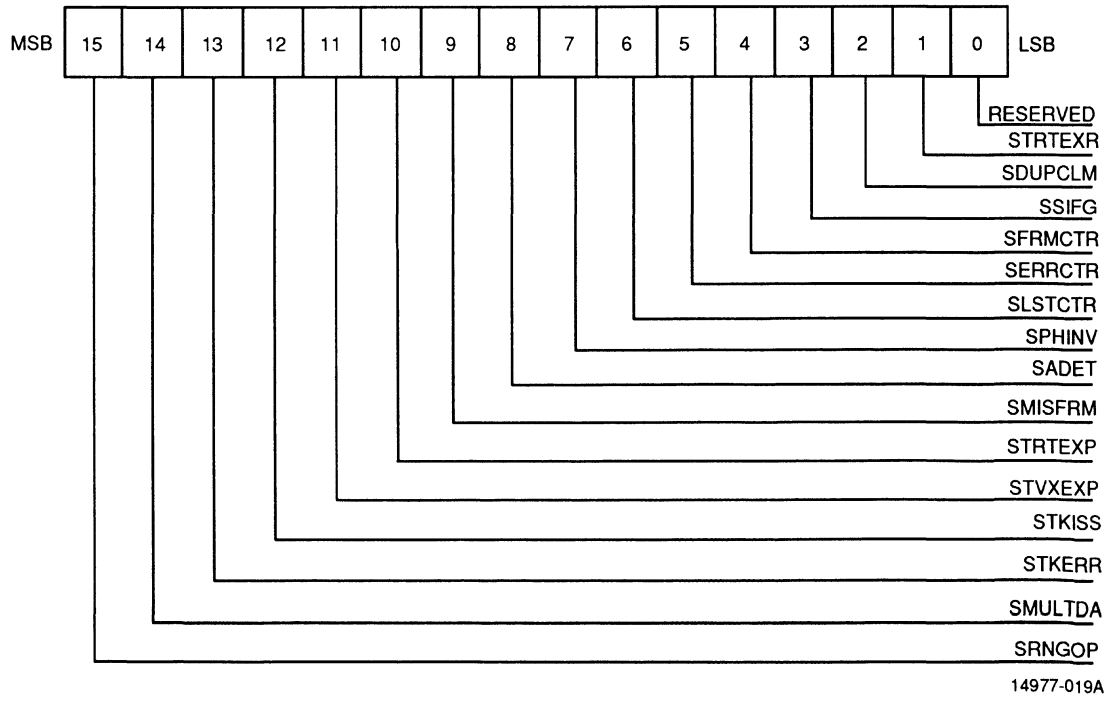


Figure 14. Status Register 2 – Lower 16 Bits (ST2L)

The following bits are in ST1U (the upper half of ST1).

Status Transmit Abort. SXMTABT (bit 15)

Status transmit abort is set when FORMAC Plus aborts a transmission by halting the transmission of data on the X-bus, as described in the following cases:

CASE 1: FORMAC Plus aborts transmission when it makes a transition from state T2 (TX_DATA) to state T0 (TX_IDLE) (i.e., reset) or from T2 (TX_DATA) to T4 (CLAIM_TK) (i.e., recovery) as defined in the FDDI standards. When it aborts transmission the corresponding queue is locked.

CASE 2: FORMAC Plus aborts transmission from the current queue on receiving a transmit-abort command via command register 2, locks the current queue, and proceeds with transmission as applicable.

CASE 3: FORMAC Plus aborts transmission from the queue in which transmit buffer underrun occurs, locks this queue, and proceeds with transmission from other queues, as appropriate. This case is applicable only to operation in tag mode.

CASE 4: Parity/Coding Errors. Note the following:

(a) Nontag mode

1. If the parity/coding errors occur in a transmit frame descriptor or a pointer, FORMAC Plus aborts transmission from that queue, locks the queue, and starts transmission from the other queues, as appropriate.
2. If a parity error occurs in the data, FORMAC Plus aborts transmission of that frame and proceeds to transmit the next frames as appropriate. In this case the queue is not locked.

(b) Tag mode

PARITY ERRORS. If a parity/coding error occurs in a buffer-memory descriptor, or a parity error occurs in the data, FORMAC Plus continues transmission of that frame until its end (i.e., until it encounters a correct long word with its tag-bit set). In this case, it does not append the FCS or end delimiter to this frame, FORMAC Plus continues transmitting other frames, and the queue is not locked.

CASE 5: When the XMTABT bit is set in the transmit descriptor in both the tag- and nontag modes, FORMAC Plus aborts transmitting this frame and continues with other frames of the queue, or other queues, as appropriate.

Note: In any of the above cases, when transmission is aborted FORMAC Plus does not append either the FCS field or the end delimiter.

Status Transmit Abort Due to Reset or Recovery (Synchronous, Async0, Async1, Async2). STXABR(S, A0, A1, A2) (bits 14–11)

One of these bits is set by the FORMAC Plus in the event of aborting a frame transmission by leaving T2 (TX_DATA) state and making a transition to T0 state (IDLE), or T4 (CLAIM_TK) state, or T5 (TX_BEACON) state in the transmit state machine (as per FDDI standards). These bits may be used during ring recovery.

Status Transmit Buffer Full, Synchronous Queue; and Status Transmit Buffer Full, Asynchronous Queues. STBFLS, STBFLA (bits 10–9) (tag mode only).

STBFLS is set when the synchronous transmit buffer is full, and STBFLA is set when any one of the three asynchronous transmit buffers is full. The buffers may become full if the host/NP does not recognize and/or act upon the almost-full status message on the QCTRL2-0 lines and then continues to assert HSREQ for buffer writes. FORMAC Plus grants HSACK in response to HSREQ requests until the buffer becomes full; then HSACK is withheld until the queue becomes available for further writes (see the discussion of Buffer Queue Control (QCTRL2-0) under Pin Description). These bits do not indicate a data-corruption or data-loss condition, only a buffer-full condition.

Status Transmit Until XDONE in Synchronous Queue. STEXDONS (bit 8)

This bit when set indicates that a frame whose descriptor has the bit XDONE set is encountered during transmission from the synchronous queue. This bit is set even when the frame is aborted. In nontag mode, the host/NP can use this information for recovering queued transmit buffers.

Status Transmit End of Chain of Frames (Synchronous, Async0, Async1, Async2). STECFRM(S, A0, A1, A2) (bits 7–4)

In the nontag bit mode, when all the frames in the chain of a transmit queue are transmitted, the corresponding STECFRM bit is set. The host/NP can use this information to add another chain to the queue. The transmit queues support at most two pending chains at any time. For tag mode these bits are not meaningful. This bit is set even when the frame is aborted.

Status Transmit End of Frame (Synchronous, Async0, Async1, Async2). STEFRM(S,A0,A1,A2) (bits 3–0)

These bits are set on the completion of a transmission for each frame in the corresponding transmit queue. These bits are not set if the frame is aborted.

The following bits are in ST1L (the lower half of ST1).

Status Transmit Buffer Underrun (Synchronous, Async0, Async1, Async2). STBUR(S, A0, A1, and A2) (bits 15–12)

These bits, in tag mode, are set when an on-chip transmit FIFO buffer underrun condition is detected during the transmission of a frame. The underrun condition causes the frame in transmission to be aborted and its queue to be locked.

Status Parity/Coding Error in Pointer, Descriptor, or Data (Synchronous, Async0, Async1, Async2). SPCEPD(S, A0, A1, and A2) (bits 11–8)

These bits are set in any of the following three conditions:

1. When the FORMAC Plus detects a parity error while reading control information such as a pointer (nontag mode only) or a descriptor.
2. When a parity error is encountered in reading buffer-memory data.
3. When there is a violation in the required coding format for a pointer (nontag mode only) or descriptor in the transmit queues.

See the discussion of Status Transmit Abort (SXMTABT in status register ST1U) for details regarding the action taken when parity/coding errors occur.

Status Transmit Instruction Full (Synchronous, Async0, Async1, Async2). STXINFL(S, A0, A1, and A2) (bits 7–4)

These bits are only used in nontag mode and indicate the full status of the transmit instruction counters (maximum count of two) for each queue. If the FORMAC Plus is currently operating on a transmit chain, the FORMAC Plus may be given and will remember another transmit chain command provided the corresponding bit is not set. FORMAC Plus ignores transmit instructions issued while the STXINFL bit is set.

Status Queue Lock (Synchronous, Async0, Async1, Async2). SQLCK(S, A0, A1, and A2) (bits 3–0)

These bits are set high on FORMAC Plus reset, or when the queues are locked by FORMAC Plus to prevent any transfer from them for transmission. These bits are reset when a queue-unlock instruction is issued through the NP.

Status Register 2 (ST2)

The ST2 register contains the status bits that may generate maskable interrupts on the $\overline{\text{MINTR2}}$ pin. ST2 contains status bits associated with receive and network operations. All status bits except SRBMT, SRBFL and SRNGOP are auto-cleared on reading the register. The remaining bits are set/reset depending upon the state of the monitored conditions.

Whenever any of the bits of status register 2 causes an interrupt on $\overline{\text{MINTR2}}$, the user must read all 32 bits of ST2 to enable any future interrupt generation.

A FORMAC Plus reset clears both the upper and lower 16-bit registers except the bit SRBMT, which retains its old value. The following paragraphs describe the functions of the bits in ST2.

The following bits are in ST2U (the upper half of ST2).

Status Receive Complete. SRCOMP (bit 15)

This bit is set at the completion of a frame reception following the writing of the frame status and length. Receive frames that are aborted set this bit, but flushed frames do not. This is valid in nontag mode only.

Status Receive Buffer Empty. SRBMT (bit 14)

This bit is set when the receive buffer is empty (i.e. RPR = WPR after an increment of RPR), and is reset when frames are in the receive buffer. This bit is not auto-cleared when read. An interrupt is generated due to setting of this bit only when a read from the receive queue is attempted while the receive buffer is empty.

Status Receive Abort. SRABT (bit 13)

The SRABT bit is set when the frame being received is aborted. Frames that normally would be flushed but are aborted due to threshold criterion in tag mode would not set this bit.

Status Receive Buffer Full. SRBFL (bit 12)

This bit is set when the receive buffer is full (RPR = WPR after an increment of WPR). The buffer-memory receive queue is then locked for further input. SRBFL can be cleared using the clear receive queue lock (20H) or clear all queue locks (3FH) commands.

Status Receive FIFO Overflow. SRCVOVR (bit 11)

This bit, when set, indicates that the FORMAC Plus receive FIFO has overflowed and receive data has been lost. This condition may occur during the receive buffer full state. FORMAC Plus will not set the frame-status C indicator (frame copied) on repeated frames when this bit is set.

Receive Frame. SRCVFRM (bit 10)

This bit is set, during single-frame receive-mode operation, to interrupt the NP and indicate that data is present in the buffer memory. The NP must then send the 'enable single frame receive' command to assert RDATA.

Receive Frame Counter Overflow. SRFRCTOV (bit 9)

The SRFRCTOV bit is set when the eight-bit receive-frame counter used in the single-frame receive mode overflows.

Status NP FORMAC Plus Simultaneous Load. SNFSLD (bit 8)

This bit is set when the NP and the FORMAC Plus simultaneously attempt to load any pointer in the FORMAC Plus. This includes all the read and write pointers that can be changed during the FORMAC Plus operation. If there is contention, FORMAC Plus has the higher priority and sets the SNFSLD bit.

Status Error In Special Frame. SERRSF (bit 7)

This bit is set when there is a parity/coding error in the descriptor of a special frame, or a parity error (nontag mode only) in the data field of a special frame. FORMAC Plus aborts transmission of any special frame (claim/beacon/auto-void) in which any of these errors is detected. However, if the special frame is a claim or a beacon frame, then FORMAC Plus repeats the transmission from the special frame's starting address (SACL or SABC, as appropriate) until the user intervenes. The SMTABT bit (tramsmit abort) in ST1U is not set.

Status Claim State Entered. SCLM (bit 6)

The SCLM bit in ST2U is set when the FORMAC Plus enters state T4 (claim state), as described in the FDDI transmit state-machine specifications.

Status My Claim. SMYCLM (bit 5)

The bit SMYCLM is set when a claim frame originated by this station is received, as per FDDI specifications.

Status Higher Claim. SHICLM (bit 4)

The SHICLM bit is set when a claim frame is received with a higher claim bid value than the one issued by this station, as per FDDI specifications.

Status Lower Claim. SLOCLM (bit 3)

The SLOCLM bit is set when a claim frame is received with a lower claim bid value than the one issued by this station, as per FDDI specifications.

Status Beacon State Entered. SBEC (bit 2)

The SBEC bit in ST2U is set when the FORMAC Plus enters state T5 (beacon state), as described in the FDDI transmit state-machine specifications.

Status My Beacon. SMYBEC (bit 1)

When a beacon frame is received with a source address equal to the address of this station (i.e. SA = MA), the bit SMYBEC is asserted.

Status Other Beacon. SOTRBEC (bit 0)

The SOTRBEC bit is asserted when a beacon frame is received with a source address not equal to the address of this station (i.e. SA ≠ MA).

The following bits are in ST2L (the lower half of ST2).

Status Ring Operational. SRNGOP (bit 15)

This bit is cleared on recovery or reset, and set after the first token is received. Any transition in SRNGOP generates an interrupt on $\overline{\text{MINTR2}}$ when not masked. This bit reflects the current operational status of the ring and is not affected by reading status register 2 (ST2L).

Status Multiple Destination Address. SMULTDA (bit 14)

When the SMULTDA bit is set, it signals the node processor that another station on the ring has the same individual address as this station. To set the SMULTDA bit, both of the following conditions must be satisfied:

1) The destination address of the received frame equals the address of this station ("my address"), i.e. DA = MA.
2) The frame-status A indicator of the received frame is in the set (S) condition when the frame is received.

Status Token Error. STKERR (bit 13)

The status token error bit (STKERR) is set due to either of the following conditions:

1) If a valid token is received while FORMAC Plus transmitter is in states T2 (Transmit Data) or T3 (Issue Token).
2) If a valid frame other than a token, and not originated by this station, is received while the FORMAC Plus is in states T2 (Transmit Data) or T3 (Issue Token). This condition is not valid for On-Line Special mode.

This bit flags a duplicate token condition.

Status Token Issued. STKISS (bit 12)

The STKISS bit is set when the FORMAC Plus issues a token and leaves the T3 (Issue Token) state.

Status TVX expired. STVXEXP (bit 11)

The STVXEXP bit is set when the FORMAC Plus TVX (expected time between valid transmissions) timer expires.

Status TRT expired. STRTEXP (bit 10)

The STRTEXP bit is set when the token rotation timer (TRT) expires and the late count is not equal to zero.

Status Missed Frame. SMISFRM (bit 9)

The SMISFRM bit is set when the destination address of a received frame equals this station's address (i.e. DA = MA) but, for some reason, this station does not set the frame-status C indicator, and repeats it as received. This signals the node processor that a frame intended for this station was not copied.

Status Address Detect. SADET (bit 8)

The SADET bit is set when a received-frame DA = MA match occurs as indicated by the internal-detection logic. The SADET bit is useful for monitoring frame reception while data is being transmitted. This status bit is also used to check the address-detect logic during loopback testing.

Status PHY Invalid. SPHINV (bit 7)

This bit is set upon receipt of the PHY-Invalid symbol from the physical-layer (PHY) receiver. PHY-Invalid is indicated by all ones on the upper nibble of the selected RA or RB bus with the upper control input line (RACU or RBCU) held high, or by all ones on the lower nibble of the selected RA or RB bus with the lower control input line (RACL or RBCL) held high.

Status Lost Counter. SLSTCTR (bit 6)

The SLSTCTR bit is set when the 16-bit Lost Counter (LCNTR) overflows.

Status Error Counter. SERRCTR (bit 5)

The SERRCTR bit is set when the 16-bit Error Counter (ECNTR) overflows.

Status Frame Counter. SFRMCTR (bit 4)

The SFRMCTR bit is set when the 16-bit Frame Counter (FCNTR) overflows.

Status Short Inter-Frame Gap. SSIFG (bit 3)

The SSIFG bit is set when the FORMAC Plus detects a short inter-frame gap (IFG) on the network. A short IFG is flagged when the gap is less than 6 bytes. FORMAC Plus can instantaneously tolerate IFGs down to 1 byte in length but whether the second frame is received or aborted depends on the available free space in the on-chip receive FIFO (see the discussion of Frame Abort under On-Line Mode). This bit can be used for network diagnostics.

Status Duplicate Claim. SDUPCLM (bit 2)

The duplicate-claim (SDUPCLM) bit is set when both of the following conditions are satisfied:

1. A valid claim frame is received with its source address and destination address equal to this station's address (i.e. DA = SA = MA).
2. The T_BID_RC value in the information block of the claim frame is not equal to the TREQ value previously set in the FORMAC Plus for this station. The existence of a claim frame with the right address but the wrong TREQ value means that an error condition exists.

Status Token Rotation Timer Expired in Recovery. STRTEXR (bit 1)

The STRTEXR bit is set when the token rotation timer (TRT) expires while the transmit state machine is in the T4 (claim) or T5 (beacon) states.

Note: Bit 0 of ST2L is reserved.

Interrupt Mask Registers (IMSK1 and IMSK2)

These two 32-bit Interrupt Mask Registers are programmed to mask interrupt generation by the bits in status registers 1 and 2. Setting a bit to 1 in IMSK1 or IMSK2 disables interrupt generation by the corresponding bit in ST1 and ST2. A FORMAC Plus reset (hardware or software) sets all the bits in both mask registers to 1. To enable any interrupt, the corresponding bit in the IMSK1 or IMSK2 register has to be reset to a 0.

DATA HANDLING AND FORMATS

Data Format of Transmit Frames In Buffer Memory

Introduction

TAG MODE. Figure 6 shows how transmit frames are queued in buffer memory in tag mode. Transmit frames always start on long-word boundaries. The frame may end at any byte boundary, as specified in the 32-bit descriptor word following the frame. See Figure 15 for the format of the descriptor. Frame data is stored with the tag-bit equal to 0, except for the last word of data and the descriptor word following the last word of data. For these two words the tag bit is set to 1. In the tag mode, parity is one bit per byte. Hence, for each long word there are four parity bits. Note that in the case of the least significant byte (BD7–BD0) the tag bit is included with the data bits for the calculation of parity. That is, in this case, parity is calculated on nine bits instead of eight.

NONTAG MODE. Figure 8 shows how transmit frames are queued in the buffer memory in nontag mode. In this mode, individual frames may be located anywhere in buffer memory. Each complete frame, however, must always consist of contiguous locations of words. Each frame has a 32-bit descriptor word (Figure 15) immediately preceding the frame, and a 32-bit pointer word (Figure 16) immediately following the frame. The descriptor includes the length of the frame in bytes. The pointer contains the address of the following frame with its descriptor word. In nontag mode, transmit frames can start on any byte of a long word (indicated by the TXFBB1-0 bits of the descriptor). The LSB bit of MDREG2 selects the order of transmission (i.e., LSByte first or MSByte first). In both tag- and nontag modes parity is one bit per byte.

Note: Except where otherwise specified, the following discussion of the transmit-frame descriptor applies to both tag- and nontag modes.

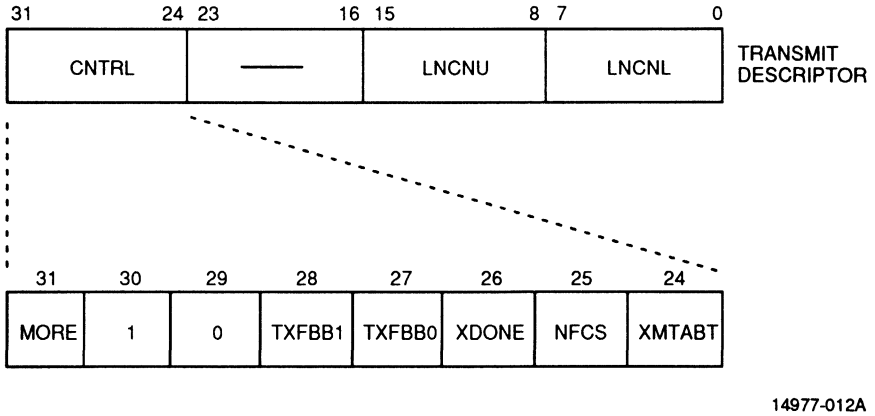


Figure 15. Format of Transmit Descriptor

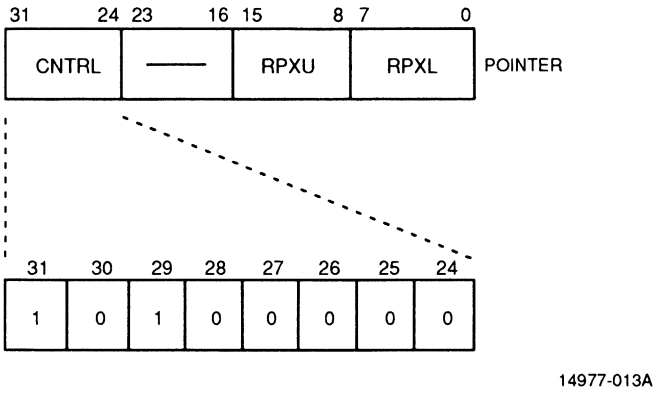


Figure 16. Format of Pointer (Nontag Mode)

Transmit Descriptor Format

Figure 15 shows the various bits of the transmit descriptor word. **Note:** Bits 30 and 29 of the descriptor word are fixed at 1 and 0 respectively. The other bits are described in the following paragraphs.

More Frames in Queue (nontag mode only). MORE (bit 31)

This bit is used to chain a group of frames for transmission in nontag mode. It indicates that there is at least one more frame in the chain following this frame. MORE, when 0, indicates that this is the last frame in the chain.

Transmit Frame Byte Boundary. TXFBB1-0 (Bits 28–27)

TAG MODE. In tag mode the two TXFBB bits provide a binary value that defines which of the four bytes of a long word contains the *last* byte in a transmit frame. Whether the location of this boundary byte is counted starting from the most-significant byte or from the least-significant byte of the long word in which it is located, is dependent upon the state of the LSB bit in mode register 2. As shown in the following table, if LSB = 0 then the bytes are counted starting from the long word's most significant byte (MSBYTE). If LSB = 1 then the bytes are counted from the least significant byte (LSBYTE).

Case 1: LSB = 0 (in MDREG2, bit 11) Tag Mode

If TXFBB1-0 =	00	01	10	11
Then last byte ends at:	Byte 1 (MSBYTE)	Byte 2	Byte 3	Byte 4 (LSBYTE)

Case 2: LSB = 1 (in MDREG2, bit 11) Tag Mode

If TXFBB1-0 =	11	10	01	00
Then last byte ends at:	Byte 4 (MSBYTE)	Byte 3	Byte 2	Byte 1 (LSBYTE)

NONTAG MODE. In nontag mode, the two TFXBB bits define the location of the *first* byte of data in a transmit frame. Note that this use of the TFXBB value in nontag mode is the opposite of that used in tag mode (see following table).

Case 1: LSB = 0 (in MDREG2, bit 11) Nontag Mode

If TXFBB1-0 =	00	01	10	11
Then first byte starts at:	Byte 1 (MSBYTE)	Byte 2	Byte 3	Byte 4 (LSBYTE)

Case 2: LSB = 1 (in MDREG2, bit 11) Nontag Mode

If TXFBB1-0 =	11	10	01	00
Then first byte starts at:	Byte 4 (MSBYTE)	Byte 3	Byte 2	Byte 1 (LSBYTE)

Transmit Done. XDONE (Bit 26)

If the XDONE bit (bit 26) in a synchronous or asynchronous frame's transmit descriptor (Figure 15) is set, FORMAC Plus, after transmitting the current frame, prevents further transmission from this queue until a new token is captured.

In the case of synchronous transmission, the setting of this bit indicates that this is the last frame transmitted during this token opportunity. This feature can be used to limit the maximum synchronous transmit time within one token opportunity. **Note**: While the XDONE bit can be similarly employed with asynchronous queues, its usage for this purpose is not recommended.

FCS or No FCS (Frame Check Sequence). NFCS (Bit 25)

If the no frame-check sequence (NFCS) bit is set to 0, then the FORMAC Plus appends a 32-bit calculated CRC frame-check-sequence value (FCS) after the transmitted frame's information block. If the NFCS bit is set to 1 then the calculated CRC frame-check-sequence value is omitted.

Transmit Abort. XMTABT (Bit 24)

If the XMTABT bit is set, it signals to the FORMAC Plus that this frame should be aborted because of some error during a transfer from system memory to buffer memory. This will not affect transmission of subsequent frames.

Bits 23-16 Reserved.

Bits 15-0: Not used in tag mode.

Length Count (In Bytes) of Next Frame. LNCNU (Bits 15-8) and LNCLN (Bits 7-0). Nontag Mode Only.

NON TAG MODE ONLY. The LNCNU and LNCNL bytes supply the length count (in bytes) of the next transmit frame. These two bytes are, respectively, the upper and lower eight bits of a 16-bit length value.

Transmit Pointer Format (Nontag mode only)

Control Byte (Bits 31–24)

Figure 16 shows the fields within the 32-bit pointer word of a nontag-mode buffer-memory frame. The first eight bits of the pointer (bits 31–24) are a fixed pattern, set at 10100000 (A0H), that act as the pointer's control byte; i.e. they uniquely identify it as a pointer.

Bits 23–16. Reserved.

Read Pointers. RPXU (Bits 15–8) and RPXL (Bits 7–0)

The read pointers RPXU and RPXL are 8-bit values that make up the upper and lower halves, respectively, of the 16-bit address for the descriptor of the next frame to be transmitted in nontag mode.

Data Format of Receive Frames In Buffer Memory

Introduction

TAG MODE. Figure 7 shows how receive frames are queued in buffer memory in tag mode. These frames are stored contiguously (i.e. like a large FIFO). Which of the four bytes of the first buffer-memory long word receives the first byte of data to be stored is defined by the states of the RXFBB1-0 bits of mode register 2 (see receive-frame byte boundary under the discussion of Mode Register 2). Whether the least-significant byte or most-significant byte of a buffer-memory long word is the starting point from which this byte is counted is determined by the state of the LSB bit in mode register 2 (MDREG2). The status and length of the received frame is stored in the long word that follows the long word containing the last byte of the frame. The tag bit is at 0 for all data words and is set to 1 only for the frame-status word at the end of the frame. In this mode of operation, the frame doesn't have to be completely received before transfer to system memory can begin. Note that because the status word is at the end of the frame, it is not available to be read until the complete frame has been read out of buffer memory.

NONTAG MODE. Figure 10 shows how receive frames are queued in the buffer memory in nontag mode. The frames are stored in buffer memory in the same manner as in tag mode. The status and length of the last received frame is stored in the long word immediately preceding the frame. The long word following this frame is always loaded with 0's. When the next frame has been completely received, the status and length of the frame is written back into this location, thus overwriting the 0's that were there. When the status is written, bit 31 of the long word now becomes a 1 to indicate a complete frame in buffer memory. Hence, in this mode, the frame has to be fully written before it can be read out.

For both the tag- and nontag modes parity is provided for each byte in buffer memory.

Note: Except as otherwise specified, the following discussion of the receive frame-status word applies to both tag- and nontag modes.

Format of Receive Status Word

The 32-bit status and length word is shown in Figure 17. The individual bits are described in the following paragraphs.

Memory Status Valid. MSVALID (Bit 31)

This bit is always a 1. Its presence in bit 31 indicates the end of a complete receive frame. In nontag mode this bit also overwrites the 0 in bit 31 that indicates the end of a queue.

Memory Status for Receive Abort. MSRABT (Bit 30)

The setting of this bit indicates that the frame was aborted during reception.

Bit 29: Reserved

Status Source Routing. SSRCRTG (Bit 28)

This bit is set if the source address (SA) of the frame has the MSB set. This feature is useful for source-routing bridges.

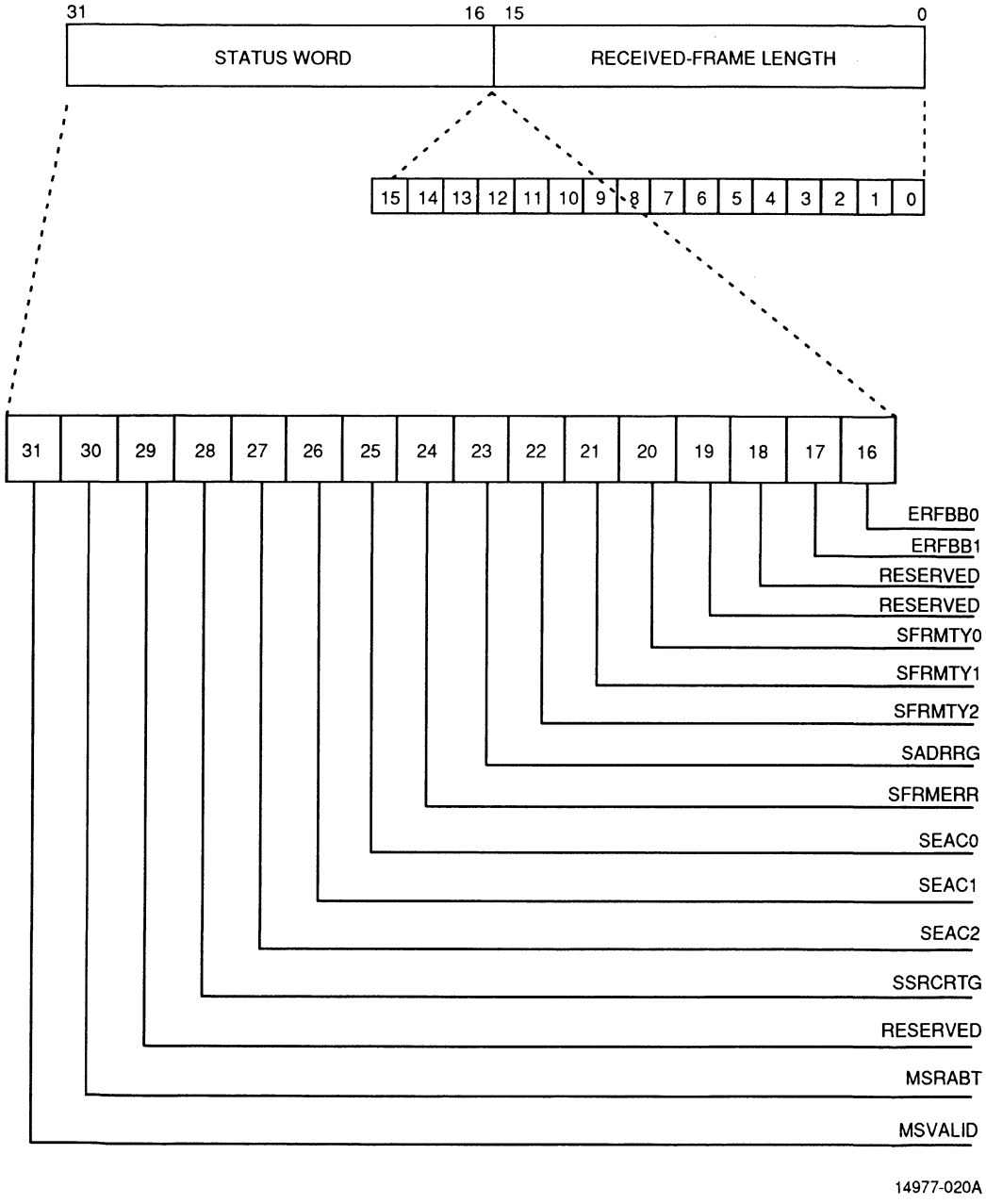


Figure 17. Receive Frame Status Word

Status of the EAC Indicators received. SEAC2-0 (Bits 27-25)

These three bits indicate the set/reset state of the three frame-status (FS) fields when received from the ring. The states of these bits provide the following information:

SEAC2: State of the frame error E-indicator.

SEAC1: State of the address match A-indicator.

SEAC0: State of the frame copied C-indicator.

The meanings of these states are given in Table 6.

Table 6. Summary of the States of the EAC Indicators (SEAC2–0).

SEAC2 State (E Indicator)	SEAC1 State (A Indicator)	SEAC0 State (C Indicator)	Meaning
0	–	–	E received as R symbol.
1	–	–	E received as non-R symbol.
–	0	0	A and C received as R symbols.
–	0	1	A received as R, and C received as S; or error in A and/or C symbols.
–	1	0	A received as S, and C received as R.
–	1	1	A and C received as S.

Legend:
R = Reset-status indicator
S = Set-status indicator

Status Frame Error. SFRMERR (Bit 24)

This bit is set if the frame received is not a valid frame (see FDDI MAC standards for definition of a valid frame) and the E indicator is received as non-R.

Status Internal Address Recognized. SADRRG (Bit 23)

This bit is set if the received frame's destination address (DA) matches any of the criteria that define this station's own 16-bit or 48-bit address (i.e. MA). Physical address, broadcast, and multicast frames set this bit when they are accepted. This bit is not set if an external address match is used to accept the frame (using the $\overline{\text{XDAMAT}}$ pin).

Status Frame Type. SFRMTY2-0 (Bits 22–20)

The states of these three bits indicate the various types of frames currently being stored in buffer memory. These states are decoded from the frame-control (FC) field of the received frame. Their meanings are given in Table 7.

Table 7. Summary of the Status Frame Type (SFRMTY2–0).

SFRMTY2 (Frame-class bit) 0 = asynchronous 1 = synchronous	SFRMTY1 (Frame-type bit)	SFRMTY0 (Frame-type bit)	Frame Type (per FDDI)
The following apply to received asynchronous frames.			
0	0	0	Void/SMT
0	0	1	LLC
0	1	0	Implementor
0	1	1	Reserved
The following apply to received synchronous frames.			
1	0	0	MAC
1	0	1	LLC
1	1	0	Implementor
1	1	1	Reserved

End of Received Frame Byte Boundary. ERFBB1-0 (bits 17–16)

The two ERFBB bits provide a binary value that defines which of the four bytes of a long word contains the last byte in a receive frame. Whether the location of this boundary byte is counted starting from the most significant byte or from the least significant byte of the long word in which it is located, is dependent upon the state of the LSB bit in mode register 2 (bit 11). As shown in the following table, if LSB = 0 then the bytes are counted starting from the long word's most significant byte (MSBYTE). If LSB = 1 then the bytes are counted from the least significant byte (LSBYTE).

Case 1: LSB = 0 (in MDREG2, bit 11)

If ERFBB1-0 =	00	01	10	11
Then last byte ends at:	Byte 1 (MSBYTE)	Byte 2	Byte 3	Byte 4 (LSBYTE)

Case 2: LSB = 1 (in MDREG2, bit 11)

If ERFBB1-0 =	11	10	01	00
Then last byte ends at:	Byte 4 (MSBYTE)	Byte 3	Byte 2	Byte 1 (LSBYTE)

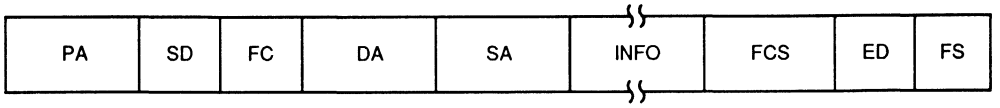
Received-Frame Length. (Bits 15–0)

The length of the frame received into the buffer memory (in bytes) includes the FC, DA, SA, INFO and FCS fields (if received into buffer memory). The length of an aborted frame is ignored.

FDDI FRAME FORMAT

The components of an FDDI frame are described in the FDDI Token Ring MAC Layer Protocol Standard. Basically, frames are composed of nine fields, in the following order (see Figure 18):

1. IDLE: Frame Preamble
2. SD: Start Delimiter
3. FC: Frame Control Field
4. DA: Destination Address
5. SA: Source Address
6. INFO: Information Field
7. FCS: Frame Check Sequence (CRC)
8. ED: End Delimiter
9. FS: Frame Status



PA – Frame Preamble. Idle Symbols (16 or more symbols)
SD – Start Delimiter: J symbol followed by K symbol (2 symbols)
FC – Frame Control Field (2 symbols)
DA – Destination Address (4 or 16 symbols)
SA – Source Address (4 or 16 symbols)
INFO – Information Field
FCS – Frame Check Sequence (8 symbols)
ED – End Delimiter: T symbol (1 symbol)
FS – Frame Status. Three symbols, made up of:
E – Frame-Error Indicator (Set/Reset)
A – Address-Recognized Indicator (Set/Reset)
C – Frame-Copied Indicator (Set/Reset)

14977-021A

Figure 18. FDDI Frame Format

TRANSMIT. For transmitted frames, FORMAC Plus precedes the transmission with the required IDLE and SD symbols. FORMAC Plus expects FC, DA, SA and INFO to be stored in the transmit buffer. If the NFCS control bit (in the transmit descriptor) is cleared, the FORMAC Plus appends the CRC result after the last byte stored in memory is presented to the ring. FORMAC Plus appends to the frame the end delimiter (ED) and frame status (FS) indicators.

RECEIVE. On receive, FORMAC Plus strips IDLE and SD before storing the frame. If programmed to buffer FCS, then the 4-byte FCS field is stored at the end of the INFO field. The first three FS set/reset indicators are stored as bits in the received frame-status field.

CONFIGURATION-STRAPPING OF FORMAC Plus PINS

NP INTERFACE MODE. FORMAC Plus has only a single pin that requires strapping. This is the NPMODE line. When this pin is strapped HIGH, NP interface operation is synchronous to BCLK. If the NPMODE pin is strapped LOW, NP interface operation is asynchronous.

PROGRAMMING THE FORMAC Plus

Table of Programmable Resources

The programming of the registers in the following table is a two-step process:

1. A register is accessed by placing its hex address on the NPADDR6-0 bus.
2. The data contained in the register is read or loaded from the NP15-0 data bus. Reading or writing is determined by the state of the R/$\overline{W}$ line. Certain registers can be accessed only during initialization mode.

USER-PROGRAMMABLE REGISTERS. The address on the NPADDR6-0 bus selects the proper programmable register for a read or write operation. The reading or writing of each register is controlled by the state of the R/W line. The data is either read onto (R = 1), or loaded from (W = 0) the 16-bit data bus (NP15-0). The following table lists the mnemonics of each programmable register; the required state of the R/W line for each load or read operation; the required NP addresses of these registers for their read and load operations; and a brief functional description of each register. The paragraphs following this table contain a detailed description of each of the bits in these user-programmable registers.

COMMAND REGISTERS. A write to command-register 1 (location 00H) and command-register 2 (location 01H) executes the instructions defined by the data on the NP15-0 bus. These instructions are used to force the FORMAC Plus into various operational states.

FORMAC Plus PROGRAMMABLE REGISTERS

Register Mnemonic	R/$\overline{W}$ 1=Read 0=Write	NPADDR6-0 (Hex)	Description
CMDREG1	0	00H	Load the command-register 1 instruction.
CMDREG2	0	01H	Load the command-register 2 instruction.
ST1U	1	00H	Read upper 16-bits of status register 1 (Read only).
ST1L	1	01H	Read lower 16-bits of status register 1 (Read only).
ST2U	1	02H	Read upper 16-bits of status register 2 (Read only).
ST2L	1	03H	Read lower 16-bits of status register 2 (Read only).
IMSK1U	0	04H	Load upper 16-bits of IMSK register 1
IMSK1U	1	04H	Read upper 16-bits of IMSK register 1
IMSK1L	0	05H	Load lower 16-bits of IMSK register 1.
IMSK1L	1	05H	Read lower 16-bits of IMSK register 1.
IMSK2U	0	06H	Load upper 16-bits of IMSK register 2.
IMSK2U	1	06H	Read upper 16-bits of IMSK register 2.
IMSK2L	0	07H	Load lower 16-bits of IMSK register 2.
IMSK2L	1	07H	Read lower 16-bits of IMSK register 2.
SAID	0	08H	Load short address – individual.
SAID	1	08H	Read short address – individual.
LAIM	0	09H	Load long address, individual (MSW of LAID).
LAIM	1	09H	Read long address, individual (MSW of LAID).
LAIC	0	0AH	Load long address, individual (middle: LAID).
LAIC	1	0AH	Read long address, individual (middle: LAID).
LAIL	0	0BH	Load long address, individual (LSW of LAID).
LAIL	1	0BH	Read long address, individual (LSW of LAID).
SAGP	0	0CH	Load short address – group.
SAGP	1	0CH	Read short address – group.
LAGM	0	0DH	Load long address, group (MSW of LAGP).
LAGM	1	0DH	Read long address, group (MSW of LAGP).
LAGC	0	0EH	Load long address, group (middle: LAGP).
LAGC	1	0EH	Read long address, group (middle: LAGP).
LAGL	0	0FH	Load long address, group (LSW of LAGP).
LAGL	1	0FH	Read long address, group (LSW of LAGP).
MDREG1	0	10H	Load the 16-bit mode register 1.
MDREG1	1	10H	Read the 16-bit mode register 1.
STMCHN	1	11H	Read the state-machine register (Read only).
MIR1	1	12H	Read upper 16-bits of 32-bit MAC Information register (MIR) value (Read only).
MIR0	1	13H	Read lower 16-bits of 32-bit MAC Information register (MIR) value (Read only).

FORMAC Plus PROGRAMMABLE REGISTERS (Continued)

Register Mnemonic	R/$\overline{W}$ 1=Read 0=Write	NPADDR6-0 (Hex)	Description
TMAX	0	14H	Load the 16-bit TMAX register.
TMAX	1	14H	Read the 16-bit TMAX register.
TVX	0	15H	Load the 8-bit TVX register with NP7-0.
TVX	1	15H	Read default 8-bit TVX register value on NP7-0 and the TVX timer up-counter value on NP15-8.
TRT	0	16H	Load upper 16-bits of the TRT timer (diagnostics only).
TRT	1	16H	Read the upper 16-bits of the TRT timer.
THT	0	17H	Load upper 16-bits of the THT timer (diagnostics only).
THT	1	17H	Read the upper 16-bits of the THT timer.
TNEG	1	18H	Read the upper 16-bits of the TNEG (TTRT value) register.
TMRS	1	19H	Read the lower 5-bits of TNEG, TRT, and THT timers. Bits 14–10 are the lower 5-bits of TNEG; bits 9–5 are the lower TRT bits; and bits 4–0 are the lower THT bits. Bit 15 is the late count. **Note:** The TNEG and TMRS registers are read-only.
TREQ0	0	1AH	Load the 16-bit TREQ0 register with the station's LSW of requested TRT.
TREQ0	1	1AH	Read the TREQ0 register.
TREQ1	0	1BH	Load the 16-bit TREQ1 register with the station's MSW of requested TRT (only the lower five bits are valid).
TREQ1	1	1BH	Read the TREQ1 register.
PRI0	0	1CH	Load the 16-bit priority register for asynchronous queue 0.
PRI0	1	1CH	Read the 16-bit priority register for asynchronous queue 0.
PRI1	0	1DH	Load the 16-bit priority register for asynchronous queue 1.
PRI1	1	1DH	Read the 16-bit priority register for asynchronous queue 1.
PRI2	0	1EH	Load the 16-bit priority register for asynchronous queue 2.
PRI2	1	1E H	Read the 16-bit priority register for asynchronous queue 2.
TSYNC	0	1FH	Load 16-bits of the TSYNC register.
TSYNC	1	1FH	Read 16-bits of the TSYNC register.

FORMAC Plus PROGRAMMABLE REGISTERS (Continued)

Register Mnemonic	R/$\overline{W}$ 1=Read 0=Write	NPADDR6-0 (Hex)	Description
Note: The following instructions relate to the loading and reading of buffer-memory-management registers.			
MDREG2	0	20H	Load the 16-bit mode register 2.
MDREG2	1	20H	Read the 16-bit mode register 2.
FRMTHR	0	21H	Load the frame threshold register.
FRMTHR	1	21H	Read the frame threshold register.
EACB	0	22H	Load end address. of claim/beacon area.
EACB	1	22H	Read end address. of claim/beacon area.
EARV	0	23H	Load end address of receive queue.
EARV	1	23H	Read end address of receive queue.
EAS	0	24H	Load end address of synchronous queue.
EAS	1	24H	Read end address of synchronous queue.
EAA0	0	25H	Load end address of asynchronous queue 0.
EAA0	1	25H	Read end address of asynchronous queue 0.
EAA1	0	26H	Load end address of asynchronous queue 1.
EAA1	1	26H	Read end address of asynchronous queue 1.
EAA2	0	27H	Load end address of asynchronous queue 2.
EAA2	1	27H	Read end address of asynchronous queue 2.
SACL	0	28H	Load the start address of claim frame.
SACL	1	28H	Read the start address of claim frame.
SABC	0	29H	Load the start address of beacon frame.
SABC	1	29H	Read the start address of beacon frame.
WPXSF	0	2AH	Load the write pointer for special frames.
WPXSF	1	2AH	Read the write pointer for special frames.
RPXSF	0	2BH	Load the read pointer for special frames.
RPXSF	1	2BH	Read the read pointer for special frames.
		2CH	———UNUSED ———
RPR	0	2DH	Load the read pointer for receive queue.
RPR	1	2DH	Read the read pointer for receive queue.
WPR	0	2EH	Load the write pointer for receive queue.
WPR	1	2EH	Read the write pointer for receive queue.
SWPR	0	2FH	Load the shadow write pointer for the receive queue.
SWPR	1	2FH	Read the shadow write pointer for the receive queue.
WPXS	0	30H	Load write pointer for synchronous queue.
WPXS	1	30H	Read write pointer for synchronous queue.
WPXA0	0	31H	Load write pointer for asynchronous queue 0.
WPXA0	1	31H	Read write pointer for asynchronous queue 0.

FORMAC Plus PROGRAMMABLE REGISTERS (Continued)

Register Mnemonic	R/$\overline{W}$ 1=Read 0=Write	NPADDR6-0 (Hex)	Description
WPXA1	0	32H	Load write pointer for asynchronous queue 1.
WPXA1	1	32H	Read write pointer for asynchronous queue 1.
WPXA2	0	33H	Load write pointer for asynchronous queue 2.
WPXA2	1	33H	Read write pointer for asynchronous queue 2.
SWPXS	0	34H	Load shadow write pointer for sync queue.
SWPXS	1	34H	Read shadow write pointer for sync queue.
SWPXA0	0	35H	Load the shadow write pointer for the asynchronous queue 0.
SWPXA0	1	35H	Read the shadow write pointer for the asynchronous queue 0.
SWPXA1	0	36H	Load the shadow write pointer for the asynchronous queue 1.
SWPXA1	1	36H	Read the shadow write pointer for the asynchronous queue 1.
SWPXA2	0	37H	Load the shadow write pointer for the asynchronous queue 2.
SWPXA2	1	37H	Read the shadow write pointer for the asynchronous queue 2.
RPXS	0	38H	Load read pointer for synchronous. queue.
RPXS	1	38H	Read read pointer for synchronous. queue.
RPXA0	0	39H	Load read pointer for asynchronous queue 0.
RPXA0	1	39H	Read read pointer for asynchronous queue 0.
RPXA1	0	3AH	Load read pointer for asynchronous queue 1.
RPXA1	1	3AH	Read read pointer for asynchronous queue 1.
RPXA2	0	3BH	Load read pointer for asynchronous queue 2.
RPXA2	1	3BH	Read read pointer for asynchronous queue 2.
MARR	0	3CH	Load the memory read address register with the 16-bit address for NP access of the buffer memory.
MARR	1	3CH	Read the 16-bit address from the MARR.
MARW	0	3DH	Load the memory write address register with the 16-bit address for NP access of the buffer memory.
MARW	1	3DH	Read the 16-bit address from the MARW.
MDRU	0	3EH	Load upper 16-bits of the memory data register with the data to be written into the buffer memory location addressed by the MARW.
MDRU	1	3EH	Read upper 16-bits of MDR. They hold the contents of the upper 16 bits of the buffer memory location pointed to by the MARR.

FORMAC Plus PROGRAMMABLE REGISTERS (Continued)

Register Mnemonic	R/$\overline{W}$ 1=Read 0=Write	NPADDR6-0 (Hex)	Description
MDRL	0	3FH	Load lower 16-bits of memory data register with the data to be written into the buffer memory location addressed by the MARW.
MDRL	1	3FH	Read lower 16-bits of MDR. They hold the contents of the lower 16 bits of the buffer memory location pointed to by the MARR.
Note: The following instructions relate to MAC counters and timers.			
FCNTR	0	41H	Load the 16-bit frame counter.
FCNTR	1	41H	Read the contents of frame counter.
LCNTR	0	42H	Load the 16-bit lost conter.
LCNTR	1	42H	Read the contents of lost counter.
ECNTR	0	43H	Load the 16-bit error counter.
ECNTR	1	43H	Read the contents of error counter.
TMSYNC	0	40H	Load upper 16 bits of TMSYNC timer from TSYNC register.
TMSYNC	1	40H	Read upper 16 bits of TMSYNC timer.

Legend:
Read command from NP: Asserted when R/$\overline{W}$ = 1.
Write (i.e. load) command from NP: Asserted when R/$\overline{W}$ = 0.

Programming the Mode Registers

The following paragraphs describe the operation and functioning of the bits in MDREG1 and MDREG2.

Mode Register 1 (MDREG1)

Mode Register 1 is used to program FORMAC Plus operational parameters. See Figure 19. All bits, with the exception of SELRA (bit 7 in discussion below), are reset to zero on the reset instruction given through command register 1. The following paragraphs define the bits in MDREG1.

Single-Frame Receive Mode. SNGLFRM (bit 15)

This mode is applicable only to tag mode. SNGLFRM, set high, allows the RDATA pin to go high on command from NP if the conditions for asserting RDATA are satisfied. This mode enables the user to examine frames and then dynamically assign buffers for the transfer out of buffer memory using the host interface. See discussion of loading and unloading single frames in tag mode, under Buffer Memory Operation. SNGLFRM, set low, enables multi-frame receive mode.

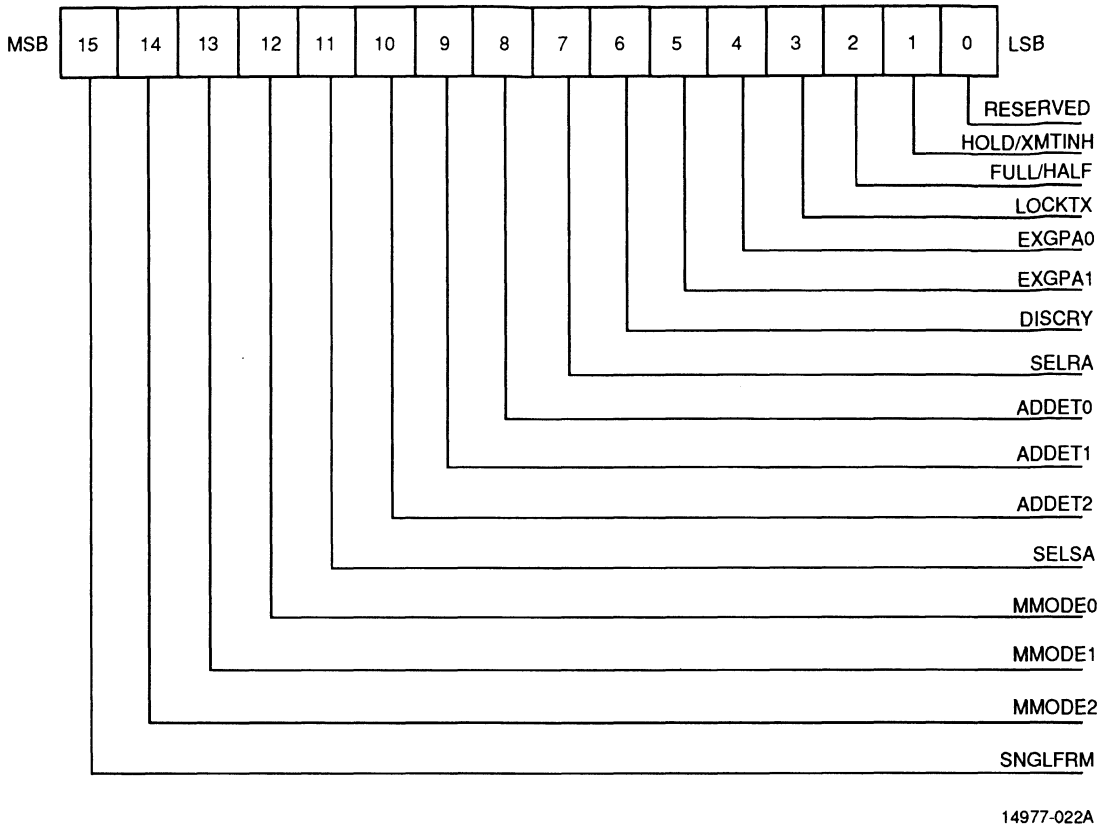


Figure 19. Mode Register 1 (MDREG1)

FORMAC Plus Operational Mode. MMODE2-0 (bits 14, 13, and 12)

The three MMODE bits control the operational mode of the FORMAC Plus. The meanings of these bit states are shown in Table 8.

Table 8. Bit assignments of the FORMAC Plus Operational Mode (MMODE2–0).

MMODE2	MMODE1	MMODE0	Description
0	0	0	INITIALIZE
0	0	1	MEMORY ACTIVE
0	1	0	ON-LINE SPECIAL
0	1	1	ON-LINE
1	0	0	INTERNAL LOOPBACK
1	0	1	RESERVED
1	1	0	RESERVED
1	1	1	EXTERNAL LOOPBACK

INITIALIZE. Initialize is the reset mode of the FORMAC Plus. In this mode, the FORMAC Plus transmit and receive state machines are held in the T0 and R0 states. Initialize mode is used to read and write FORMAC Plus internal registers. The address registers and TREQ register can only be written during the initialization mode. To ensure proper timer values before and during operation, default values for TVX and TMAX should only be written during initialization mode. When the MMODE bits are reprogrammed to exit the initialize mode, the timers TVX and TRT are loaded with their default values. **Note:** If the address registers and TREQ register are written during normal operation, the contents do not get updated.

MEMORY ACTIVE. After the internal registers have been initialized while in INITIALIZE mode, MEMORY ACTIVE mode is entered for the downloading of special frames (claim/beacon) into the special-frame area. No frames are received nor can the FORMAC Plus transmit while in MEMORY ACTIVE mode. After the special frames have been downloaded, FORMAC Plus may enter the ON-LINE state. This mode could be used to redefine the buffer memory management registers.

ON-LINE SPECIAL. This mode is same as ON-LINE MODE except that the A and C indicators are not set on receiving an external destination address match and valid copy.

ON-LINE MODE. ON-LINE MODE places the FORMAC Plus in the FDDI operational mode. The chip is enabled to receive and process data received from the selected RA or RB bus as per the FDDI protocol. On-Line operation is discussed in detail under FORMAC Plus Operational Modes

INTERNAL LOOPBACK. This setting places the FORMAC Plus in internal loopback mode. In this mode, the internal transmit bus is connected to the internal receive path. RA or RB bus inputs are ignored. The first four bytes of the information field (immediately following the SA field) of the frames transmitted during loopback will also be stored in the MIR. The NP can read these bytes to verify operation without having to read the frame stored in buffer memory.

EXTERNAL LOOPBACK. This setting places the FORMAC Plus in external loopback mode. This mode is similar to internal loopback except the loopback path is assumed to be connected outside of the chip boundary. The first four bytes of the information field following the SA field of the frames transmitted during loopback will be stored in the MIR. The NP can read these bytes to verify operation.

Select Short Address. SELSA (bit 11)

This mode bit is used by FORMAC Plus in the token claiming process. This bit should be set to 1 if the addresses transmitted in the station's claim frames are 16-bits long (i.e. 48-bit addressing is not used). Otherwise, SELSA is reset.

Address Detect. ADDET2-0 (bits 10, 9, and 8)

The ADDET bits select the conditions which inhibit the flushing of a frame during frame reception and disable receive function. These bits are decoded in Table 9.

Table 9. Bit assignments of the Address Detect (ADDET2–0)

ADDET2	ADDET1	ADDET0	DESCRIPTION
0	0	0	Receive Frames with DA = MA.
0	0	1	Receive frames with DA = MA or SA = MA.
0	1	0	Receive non-NSA frames with DA = MA and SA ≠ MA; or receive NSA frames with A=Reset and DA = MA.
0	1	1	Receive non-NSA Frames with DA = MA; or receive NSA frames with A = Reset and DA = MA.
1	0	0	Disable receive (DISRCV) function.
1	0	1	Reserved.
1	1	0	Limited-Promiscuous mode. Receive all frames except null beacon frames; claim frames; and frames with SA = MA and DA ≠ MA.
1	1	1	Promiscuous mode. Receive all frames including claim frames and void frames. Void frames are not received in any mode except the promiscuous mode.

The following paragraphs describe the various states of the ADDET2-0 bits shown in the previous table:

1. ADDET2-0 = 000: FORMAC Plus flushes the received frame when the destination address of the frame does not match the corresponding station address in the FORMAC Plus, and the $\overline{\text{XDAMAT}}$ input is not asserted (see $\overline{\text{XDAMAT}}$ timing diagram, Figure 34). Broadcast frames are treated as address matches and are always accepted. DA equals MA when DA matches either (1) the long or short individual address, or (2) the long or short group address.
2. ADDET2-0 = 001: In this mode, in addition to inhibiting the flushing of frames whose DA = MA, FORMAC Plus does not flush the frames it transmitted.
3. ADDET2-0 = 010: FORMAC Plus receives the non-NSA frames that are addressed to this station but not transmitted by this station, as well as NSA frames addressed to this station with their A indicator reset.
4. ADDET2-0 = 011: In this mode FORMAC Plus receives the non-NSA frames that are addressed to this station, as well as NSA frames addressed to this station with their A indicator reset.
5. ADDET2-0 = 100: The ADDET bits 2–0 in the state 100 produces the disable-receive (DISRCV) condition. In this state, FORMAC Plus does not receive frames from the network. The C indicators associated with address-recognized valid frames are repeated without modification when the receiver is disabled. If DISRCV is set when the FORMAC Plus is receiving a frame, the frame is aborted. No frame will be received until DISRCV is cleared.
6. ADDET2-0 = 110: This is the "limited-promiscuous" mode. In this mode, all frames, regardless of destination-address match (either internal or external), are received and not flushed, except for null beacon frames, claim frames and frames that are transmitted from this station but addressed to other stations.
7. ADDET2-0 = 111: This is the "promiscuous" mode. In this mode, all frames regardless of destination-address match (either internal or external) are received and not flushed, including claim frames and void frames. This is the only mode in which void frames can be received. **Note:** In this mode the 'Strip FCS' feature should not be used for receiving a frame.

IMPORTANT. The $\overline{\text{XSAMAT}}$ and/or $\overline{\text{XDAMAT}}$ signals must be activated as shown in their timing diagram, Figure 34, if the external address-match criterion is to be used to prevent flushing. See the discussion of Special Functions under FORMAC Plus Operational Modes for more details about $\overline{\text{XSAMAT}}$ and $\overline{\text{XDAMAT}}$ timing.

Select RA Bus or RB Bus. SELRA (bit 7)

SELRA controls the mux input to the FORMAC Plus at its interface with the PHY sublayer (per FDDI). A 1 in this bit position selects the RA bus as the active FORMAC Plus media input. A 0 selects the RB bus as the active input. SELRA retains its state after a FORMAC Plus hardware and software reset.

Disable Carry. DISCRY (bit 6)

The DISCRY bit, when set, permits testing of the operation of certain internal FORMAC Plus timers by dividing each one into independent counters of four or five bits in length. These individual small counters are then tested. By dividing them up, their full-count period during tests does not take up an undue length of time. The DISCRY bit must always be cleared in order to permit normal FORMAC Plus operation. Setting this bit breaks the TRT, THT, TVX, and TMSYNC timers into the segments shown in Table 10.

Table 10. Summary of the Disable Carry, (DISCRY) Bit Operation on FORMAC Plus Timers.

Counter Mnemonic	Normal Size with DISCRY Low	No. and Size of Counter Segments with DISCRY High	Bits Used For Each Segment
TRT	21 bits	1 segment: 5 bits 4 segments: 4 bits each	20 through 16. 15 thru 12; 11 thru 8; 7 thru 4; and 3 thru 0.
TVX	8 bits	2 segments: 4 bits each	7 thru 4; and 3 thru 0.
THT	21 bits	1 segment: 5 bits 4 segments: 4 bits each	20 through 16. 15 thru 12; 11 thru 8; 7 thru 4; and 3 thru 0.
TMSYNC	21 bits	1 segment: 5 bits 4 segments: 4 bits each	20 through 16. 15 thru 12; 11 thru 8; 7 thru 4; and 3 thru 0.

Notes:

1. In this mode, the independent timer segments clock each BCLK cycle.
2. With DISCRY set, all counter segments count continuously; i.e. they wrap around.
3. DISCRY, when set, overrides any hold function on the timers.

Extended Group Addressing. EXGPA1-0 (bits 5–4)

These bits allow the reception of multicast frames based on the partial-address filtering shown in Table 11.

Table 11. Summary of the Extended Group Addressing (EXGPA1–0) Bits Assignments for Partial Address Filtering.

EXGPA1	EXGPA0	Partial-Address Filtering Mode
0	0	Frames with my group address accepted.
0	1	Soft Filtering. Accepts all frames with group address bit set.
1	0	Only upper 24 bits of group address register must match for multicast.
1	1	Only upper 16 bits of group address register must match for multicast.

Note:

Broadcast frames are received under all values of EXGPA1-0.

Lock Transmit Asynchronous Queues. LOCKTX (bit 3)

This bit, when low, allows all the asynchronous queues for transmission to be transparently transmitted after the completion of a ring-recovery operation. This bit, when high, forces the asynchronous transmit queues to become locked on a transition of SRNGOP, and to remain locked until the unlock command is issued. It is to be noted that the synchronous-frame queue is always locked on a transition of SRNGOP and remains locked until the unlock command is issued.

Full/Half Duplex. FULL/HALF (bit 2)

The full/half bit selects between full-duplex and half-duplex operation. This bit, when low, forces half-duplex operation. When high, it enables full duplex mode. In half-duplex mode, no received frames are buffered to memory during transmission. In full-duplex mode, depending on the state of the ADDET2-0 bits, the frames received on the RA or RB bus are buffered into memory even during transmission. This includes performing a CRC check on received frames during transmission.

Hold/Transmit Inhibit. HOLD/XMTINH (bit 1)

The FORMAC Plus HOLD/XMTINH pin can be programmed to perform either of two functions: it can provide a suspend/resume function for the chip (i.e. HOLD); or it can provide an unconditional transmit-inhibit function (i.e. XMTINH). Which of these two functions is selected depends upon the state of the HOLD/XMTINH bit.

When this bit is set high, the HOLD/XMTINH pin is selected for the transmit-inhibit function (XMTINH). When this bit is low, the HOLD function is selected. The functions of the HOLD/XMTINH pin and HOLD/XMTINH bit are described in Table 12.

Table 12. Summary of HOLD/XMTINH (bit 1) and HOLD/XMTINH Pin Functions.

HOLD/XMTINH (bit 1)	HOLD/XMTINH Pin	Function
0	0	Normal FDDI operation.
0	1	FORMAC Plus operation is suspended. All timers and state machines are frozen.
1	0	Normal FDDI operation.
1	1	All transmission inhibited but timers and state machines operate normally.

Mode Register 2 (MDREG2)

Mode register 2 is used to program buffer-memory interface operational parameters. See Figure 20. All bits are reset to zero on a reset instruction or when $\overline{RST}$ is asserted low. The following paragraphs describe the bits in MDREG2.

Buffer-Memory Mode. BMMODE (bit 15)

This bit defines whether data in buffer memory is to be stored in accordance with the tag mode format or the nontag mode format. When BMMODE = 1, tag mode is selected. When BMMODE = 0, nontag mode is selected. In tag mode (i.e. when BMMODE = 1) each frame consists of a group of long words of data followed by a status word identified by a tag bit. The nontag mode supports link-lists (as supported by the previous generation of FORMAC) for transmit frames. Receive frames are always stored in buffer memory in a FIFO mode.

Strip Frame Check Sequence (FCS). STRPFCS (bit 14)

When this bit is set high, FORMAC Plus strips the four-byte FCS field of the received frame (i.e. containing the 32-bit CRC value). When this bit is set low, FORMAC Plus includes the four-byte FCS field in the received frame in buffer memory. **Note**: This bit should not be set when receiving error frames, i.e. when RCVERR = 1.

Check Parity. CHKPAR (bit 13)

If CHKPAR is set high, the parity of the 32-bit buffer-memory BD-bus data is checked against the BDP-bus value by the FORMAC Plus during buffer-memory reads, and the parity of the BD-bus is generated and written on the BDP-bus during buffer-memory writes.

Any parity error during buffer-memory read operation while transmitting frames is flagged by the parity bits SPCEPD(S, A0, A1, and A2) in status register 1.

If CHKPAR is low, then parity is neither generated nor checked at the buffer memory interface. When CHKPAR is low:

1) The BDP bus is ignored during memory reads.
2) If SYMCTL and CHKPAR are both low, the BDP bus is forced to all-low during memory writes.
3) If SYMCTL is high and CHKPAR is low, then the BDP-bus is forced to all-high during memory writes.

Refer to the discussion of SXMTABT (status transmit abort), bit 15 of status register 1, for actions taken if parity/coding errors are detected in the transmit-queue data for both the tag- and nontag modes.

Parity Type. PARITY (bit 12)

When this bit is set high, even-parity is selected. Parity is computed on a byte basis in both the nontag mode and the tag mode.

Least Significant Byte. LSB (bit 11)

LSB high indicates that the least significant byte in a long word is transmitted/received first. The most significant byte is transmitted/received first when LSB is set low. The order of bits in a byte is not changed by the state of the LSB bit. This bit applies to frame data only and does not affect pointers, descriptors, or status words.

Receive Frame Byte Boundary. RXFBB1-0 (bits 10–9)

These bits indicate in which of the four bytes of a buffer-memory long word the loading of the received frame should begin. This is shown in the following table. Since frames can have any length, the frame may end on any boundary. The next frame is again loaded at the byte boundary indicated by RXFBB1-0. If these bits are changed during reception the results are undefined. As shown in the following table, the state of the LSB bit controls the order in which the bytes are stored in the buffer-memory long words.

Case 1: LSB = 0 (in MDREG2, bit 11)

If RXFBB1-0 =	00	01	10	11
Then first byte starts at:	Byte 1 (MSBYTE)	Byte 2	Byte 3	Byte 4 (LSBYTE)

Case 2: LSB = 1 (in MDREG2, bit 11)

If RXFBB1-0 =	11	10	01	00
Then first byte starts at:	Byte 4 (MSBYTE)	Byte 3	Byte 2	Byte 1 (LSBYTE)

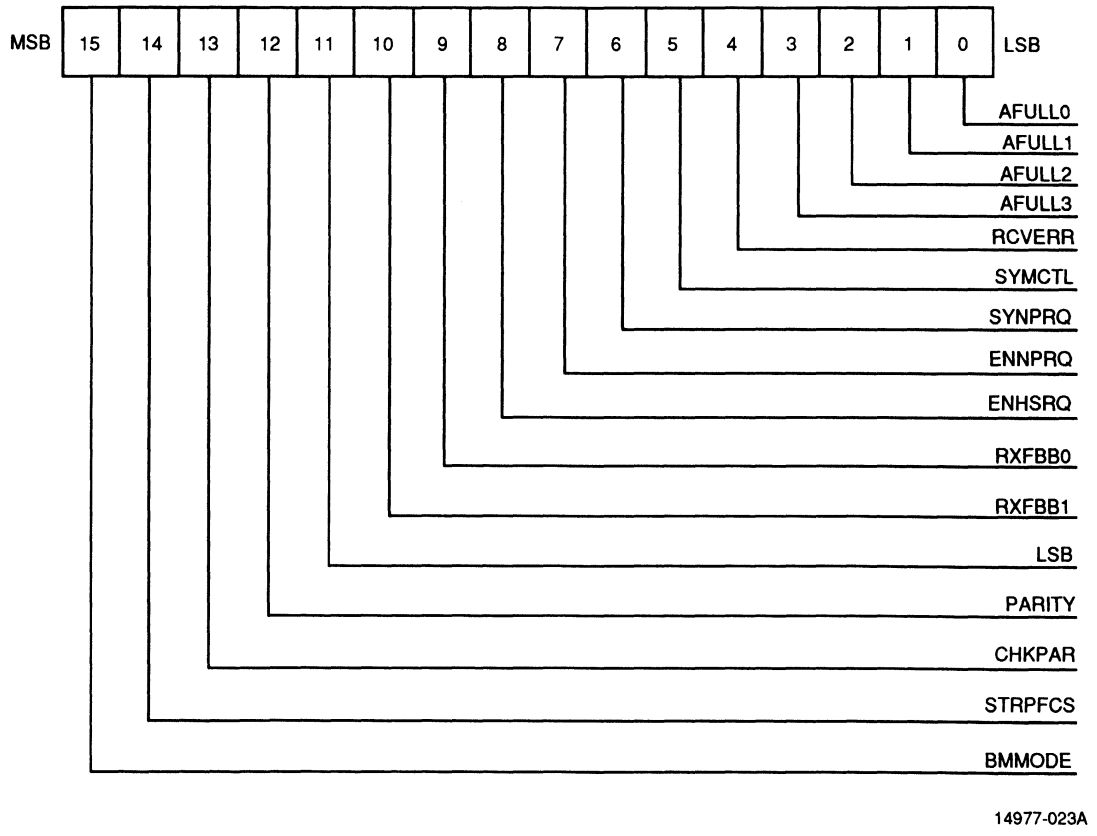


Figure 20. Mode Register 2 (MDREG2)

Enable Host Requests. ENHSRQ (bit 8)

When the FORMAC Plus is reset, this bit is reset, causing host requests to be ignored. When the ENHSRQ bit is set, host DMA requests are then detected and serviced by FORMAC Plus. Resetting ENHSRQ to a low does not affect an already acknowledged request but does disregard any pending host request. By its ability to regulate the flow of host requests, this bit can be used to control the bus-bandwidth allowed to host read/write operations by the NP.

Enable NP DMA Requests. ENNPRQ (bit 7)

On a FORMAC Plus reset, this bit is reset and disables NP DMA requests. When set, it enables this request. NP DMA requests use the NPMEMREQ and NPMEMACK signals for control of address and data buses.

Synchronous NP DMA Requests. SYNPRQ (bit 6)

When this bit is set, FORMAC Plus assumes that NP DMA requests are synchronous to BMCLK and that they satisfy setup and hold timing requirements. When SYNPRQ is reset to zero, FORMAC Plus assumes that NP DMA requests are asynchronous, and synchronizes the request within the chip. On a general FORMAC Plus reset SYNPRQ is reset to zero. In the asynchronous mode (i.e. SYNPRQ = 0), an additional clock period is needed to synchronize the request, as compared to the synchronous mode.

Symbol Control. SYMCTL (bit 5)

To use this mode, parity must be disabled by setting CHKPAR low. SYMCTL is used only for diagnostic purposes to transmit user-controlled symbols and symbol violations to the PHY (physical layer). Symbol control mode can be used in both tag and nontag modes.

When the SYMCTL bit is set high and a word is written to buffer memory by the NP using the MDR registers, the parity bits BDP3-0 are all set to 1. When the SYMCTL bit is set low, the parity bits BDP3-0 are all set to zero if the CHKPAR bit is set low.

Control and data symbols may be assembled together in a frame by toggling SYMCTL during NP writes to buffer memory through the MDR registers. Data symbols have BDP3-0 = 0000 and control symbols have BDP3-0 = 1111. To write data symbols through MDR, SYMCTL must be set low. Using the NP write operation through the MDR, control and data symbols can be assembled on a long word "granularity" only, i.e. a word can contain either control symbols or data but not both. See the discussion on Command Registers 1 and 2 and their instruction set (below).

During transmission in symbol-control mode, each of the parity bits (BDP3-0) is routed to the XCU and XCL paths, forcing the bytes written in symbol-control mode to be interpreted as control symbols if the parity bit is high, or as data symbols if the parity bit is low.

SYMCTL must be set high during transmission for routing BDP3-0 to XCU and XCL. The receiver must be disabled in SYMCTL mode by setting the ADDET2-0 bits in mode register 1. No start delimiter or FCS field or end delimiter is transmitted in this mode unless the appropriate symbols are written into buffer memory.

Receive Errored Frames. RCVERR (bit 4)

RCVERR, when set to a 1, allows all frames that pass the address-match conditions to be buffered to memory, even if they contain FCS-, minimum-length, or odd-byte-boundary errors, or the E indicator is not reset. The RCVERR bit set to a 0 flushes/aborts receive frames that contain errors. See the discussion of frame flushing and frame abort under On-Line Mode. The "Strip FCS" feature should not be used when this bit is set.

Almost Full. AFULL3-0 (bits 3–0)

The almost-full bits (AFULL3-0) are presettable to a 4-bit binary value representing the number of empty locations remaining in the current transmit queue. Then, during tag mode, when the number of free long words in the transmit queue currently being loaded decreases to less than twice the value programmed in AFULL3-0, FORMAC Plus signals to the host, by means of the QCTRL2-0 pins, the almost-full condition in the queue. This is used to stop loading the transmit FIFO before the queue overflows. If this function is desired, AFULL3-0 must be programmed with a non-zero value.

Command Registers 1 and 2 and Their Instruction Set

INTRODUCTION. In certain instances, the NP address bus (NPADDR6-0) and the NP instruction bus (NP15-0) are used to provide direct control of FORMAC Plus operation by issuing instructions to either of its two command registers. These registers provide a repertoire of 29 instructions affecting various aspects of chip operation. The instruction set available with these two registers is summarized in the table below, and is described in the paragraphs following the table:

Instruction Name	NP15-0 Instruction Code (Hex)	Mnemonic
Command Register 1 (NPADDR6-0 = 00H)		
Software Reset	01H	
Load MDR from buffer memory with MARR increment	02H	IRMEMWI
Load MDR from buffer memory without MARR increment	03H	IRMEMWO
Idle/Listen	04H	
Claim/Listen	05H	
Beacon/Listen	06H	
Load TVX timer from TVX register	07H	
Nonrestricted Token Mode	08H	
Enter Nonrestricted Token Mode	09H	
Enter Restricted Token Mode	0AH	
Restricted Token Mode	0BH	
Send Unrestricted Token	0CH	
Send Restricted Token	0DH	
Enter Send-Immediate Mode	0EH	
Exit Send-Immediate Mode	0FH	
Clear Synchronous Queue Lock	11H	
Clear Asynchronous Queue 0 Lock	12H	
Clear Asynchronous Queue 1 Lock	14H	
Clear Asynchronous Queue 2 Lock	18H	
Clear Receive Queue Lock	20H	
Clear All Queue Locks	3FH	
Command Register 2 (NPADDR6-0 = 01H)		
Transmit Synchronous Queue	01H	
Transmit Asynchronous 0 Queue	02H	
Transmit Asynchronous 1 Queue	04H	
Transmit Asynchronous 2 Queue	08H	
Abort Current Transmit Activity	10H	
Reset Transmit Queues	20H	
Set Tag bit	30H	
Enable Receive Single Frame	40H	

Command Register 1 (NPADDR6-0 = 00H)

Command register 1 is selected by the address 00H on the NPADDR6-0 bus. Command register 1 issues commands to FORMAC Plus to go into various operational modes and to perform certain other functions, as described below. Each function or operation is selected by the command code on the NP15-0 data bus.

Software Reset (NP15-0 = 01H)

Software reset performs the same function as asserting the $\overline{RST}$ pin. Software reset places the FORMAC Plus internal registers and state machines into a known state. FORMAC Plus goes to initialization mode on receiving a software reset. The SELRA bit in mode register 1 is not disturbed and retains its previous setting.

Load Memory Data Register (MDR) From Buffer Memory With MARR Increment. IRMEMWI (NP15-0 = 02H)

This instruction loads the MDR with the contents of the location in the buffer memory addressed by the contents of the MARR. After the buffer memory is read, the MARR is incremented. Once both the MDRL and MDRU registers are read, the data from the next location as addressed by MARR is fetched automatically. Automatic data fetching is repeated until the 'Load MDR from buffer memory without MARR increment' instruction (03H) is issued by the node processor.

Load Memory Data Register (MDR) From Buffer Memory Without MARR Increment. IRMEMWO (NP15-0 = 03H)

This instruction (03H) loads the MDR with the contents of the location in buffer memory addressed by the contents of the MARR. After buffer memory is read, the MARR is not incremented.

Idle/Listen (NP15-0 = 04H)

IDLE/LISTEN places the FORMAC Plus transmit state machine in the IDLE (T0) state while the receiver enters the LISTEN (R0) state. This function is referred to as a MAC_reset in the FDDI specification. Note that register values are unaffected by this operation.

Claim/Listen (NP15-0 = 05H)

This command forces the FORMAC Plus into the claim state. The TRT is loaded with TMAX value when this instruction is given. This corresponds to the R0 and T4 states in the FDDI specification.

Beacon/Listen (NP15-0 = 06H)

This command forces the beacon state. The TRT is loaded with TMAX when this instruction is given. This corresponds to the R0 and T5 states in the FDDI specification.

Load TVX Timer From TVX Register (NP15-0 = 07H)

On giving this command to FORMAC Plus, the value of the TVX register is loaded into the TVX timer. It is useful for testing purposes only, and should not be used in normal operation.

Restricted and Nonrestricted Transmit Modes

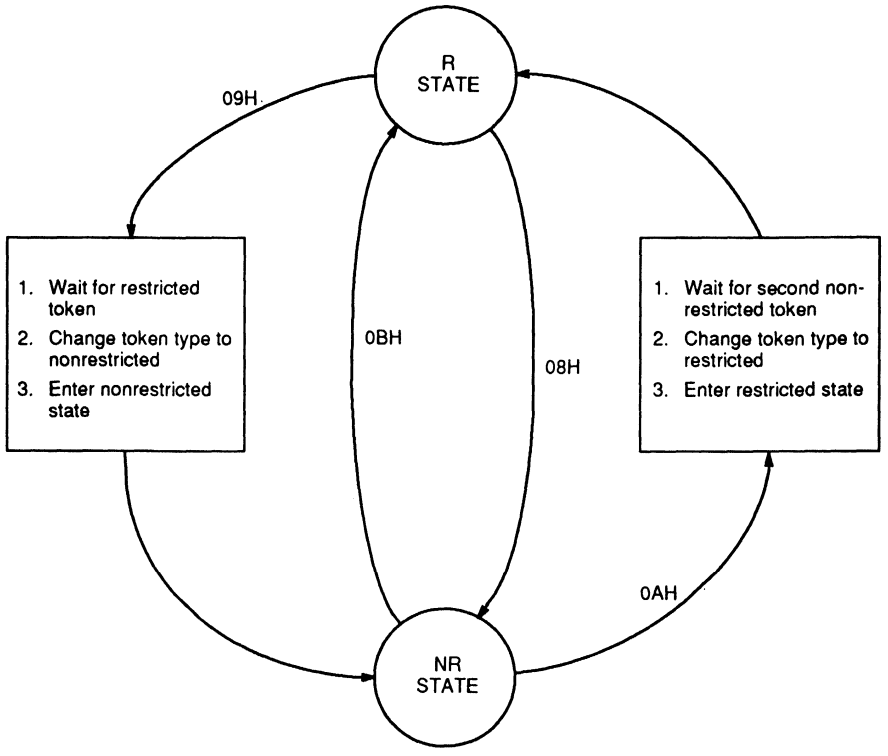
The following four commands (**08H**, **09H**, **0AH**, and **0BH**) deal with restricted and non restricted transmit modes, i.e. the modes associated with restricted and nonrestricted tokens. Before discussing these commands, it is necessary to understand the interaction of these modes with synchronous and asynchronous queues. These modes, the associated token types, and the corresponding queues that can be transmitted are shown in Table 13. See Figure 21 for a state diagram showing these modes.

Table 13. Summary of Allowed Transmission Queues with Respect to Different Token Mode and Token Type

FORMAC Plus Token Mode	Token Type	Queues That Can Be Transmitted with Indicated Mode and Token-Type
R	R	Asynchronous and synchronous
R	NR	Asynchronous and synchronous
NR	R	Synchronous only
NR	NR	Asynchronous and synchronous

Legend:
R = Restricted
NR= Nonrestricted

Notes:
1. Regardless of mode type or token type, synchronous queues can always be transmitted.
2. A nonrestricted token is defined as one that always permits transmission of both asynchronous queues and synchronous queues; i.e. it is a token that imposes no restrictions. This is true regardless of whether FORMAC Plus is in restricted or nonrestricted mode.
3. A restricted token is one that allows transmission of asynchronous queues while the FORMAC Plus is in the restricted-token mode; but only allows transmission of synchronous queues when FORMAC Plus is in non-restricted-token mode.
4. Restricted-token mode allows transmission of both synchronous and asynchronous queues when either type of token is captured.
5. Nonrestricted-token mode allows transmission of synchronous queues only, with restricted tokens; and transmission of both types of queues with nonrestricted tokens.



Legend:

R = Restricted
NR = Nonrestricted
08H = Nonrestricted token mode.
09H = Enter nonrestricted token mode.
0AH = Enter restricted token mode.
0BH = Restricted token mode.

14977-024A

Figure 21. State Diagram for Interaction of Restricted and Nonrestricted Token Modes

Nonrestricted Token Mode (NP15-0 = 08H)

This is the default option selected at chip-reset, transmit-reset, or ring-recovery. In this mode FORMAC Plus reissues the same type of token as that captured. In this mode, FORMAC Plus transmits asynchronous data only when a non-restricted token is received. Synchronous data, however, is transmitted on any token regardless of its type.

Enter Nonrestricted Token Mode (NP15-0 = 09H)

This command introduces an intermediate state between restricted and nonrestricted modes. See Figure 21. This state is selected by session-terminator (i.e. higher-level protocol) software as a method for completing a restricted dialogue. Command 09H causes a two-step operation to take place, as follows:

1. Asynchronous requests capture and use a restricted token if the criteria for THT and late-count are met.
2. In the second step of this mode FORMAC Plus issues a nonrestricted token. Once this token is issued, FORMAC Plus returns to the nonrestricted-token mode.

Enter Restricted Token Mode (NP15-0 = 0AH)

This command (0AH) places the FORMAC Plus in an intermediate mode between nonrestricted and restricted modes. See Figure 21. This option is used by higher-level protocol software when it issues command 0AH to initiate a restricted dialogue. The command takes place in two steps:

1. When the command 0AH is issued while the FORMAC Plus is in the nonrestricted-token mode, it enters an intermediate state in which it waits for the second nonrestricted (NR) token to be issued. This extra-token delay allows other stations on the ring to transmit frames before a restricted dialog can begin.

2. After the second NR token is received, the token is reissued as restricted. FORMAC Plus now enters restricted mode and a restricted-token dialog can now take place until terminated by the higher-level protocol software and the issuance of the Enter Nonrestricted Token Mode (09H) command.

Note: In the restricted-token mode, FORMAC Plus transmits a void frame (from location 0000) every time a restricted token is received and no data is queued for transmission. In restricted mode, this void frame causes the TVX of the stations on the ring to be reset in the absence of frames, since restricted tokens do not reset the TVX timers.

Restricted-Token Mode (NP15-0 = 0BH)

This mode is automatically entered on successful completion of the enter-restricted-mode instruction (0AH) described above. Restricted mode command (0BH) is also issued explicitly by other participants in the restricted dialogue once they are notified that the process has begun. In this mode, an asynchronous queue is enabled to capture and use a restricted token. Each token issued is the same type as the captured token.

Send-Immediate Commands

The following three commands can be used to force immediate transmission on the media:

1) Send nonrestricted token (0CH).

2) Send restricted token (0DH).

3) Enter send-immediate mode (0EH).

It is important to note that while these commands are required by the FDDI standards they are not intended for normal operation and should only be used under rare circumstances. Issuing these instructions causes a transmit reset as outlined in the FDDI Transmit State Machine. This has the effect of setting T_OPR to T_MAX, loading TRT with T_OPR and clearing the SRNGOP bit in the status register. See the discussion of send-immediate mode under Buffer-Memory Operation.

Send Nonrestricted Token (NP15-0 = 0CH)

This option resets the FORMAC Plus transmitter and then causes a transition to the T3: Issue_Token state. A nonrestricted token is subsequently issued. The send instruction is cleared after the token has been sent.

Send Restricted Token (NP15-0 = 0DH)

This option resets the FORMAC Plus transmitter and then causes a transition to the T3: Issue_Token state. A restricted token is subsequently issued. The send instruction is cleared after the token has been sent.

Enter Send-Immediate Mode (NP15-0 = 0EH)

On giving the command 0EH, FORMAC Plus enters the send-immediate mode and operates for transmission without capturing a token. Bit 12 in the state machine register is set high as long as the FORMAC Plus is operating in send-immediate mode. When this command is given in the middle of a frame transmission the ring goes nonoperational, the frame being transmitted is aborted, and the queue is locked. As soon as this command is decoded by FORMAC Plus, TRT is loaded with TMAX.

Exit Send-Immediate Mode (NP15-0 = 0FH)

On giving this command the FORMAC Plus exits the send-immediate mode and bit 12 in the state machine register is reset. After exit, FORMAC Plus goes to the X_IDLE (T0) and LISTEN (R0) states. After this command is decoded, the SRNGOP bit in ST2L is reset.

Clear Sync Queue Lock (NP15-0 = 11H)

This instruction clears a lock on the synchronous transmit queue.

Clear Async0 Queue Lock (NP15-0 = 12H)

This instruction clears a lock on asynchronous transmit queue 0.

Clear Async1 Queue Lock (NP15-0 = 14H)

This instruction clears a lock on asynchronous transmit queue 1.

Clear Async2 Queue Lock (NP15-0 = 18H)

This instruction clears a lock on asynchronous transmit queue 2.

Clear Receive Queue Lock (NP15-0 = 20H)

This instruction clears a lock on the receive queue to enable further transfer of data received from the receive FIFO. It also clears the receive buffer full (SRBFL) bit in status register 2 (bit 12 of ST2U).

Clear All Queue Locks (NP15-0 = 3FH)

This instruction clears locks on all queues.

Command Register 2 (NPADDR6-0 = 01H)

Command Register 2 includes commands to FORMAC Plus to transmit from a specific queue in nontag mode. FORMAC Plus supports a maxmimum of two chains in a transmit queue. The various commands available through command register 2 are described in the following paragraphs.

Transmit Synchronous Queue (NP15-0 = 01H)

This command instructs FORMAC Plus to enable the synchronous queue for transmission in nontag mode.

The synchronous queue is enabled for transmission until a frame whose descriptor has its MORE bit reset is encountered.

Transmit Asynchronous Queue 0 (NP15-0 = 02H)

This command instructs FORMAC Plus to enable asynchronous queue 0 for transmission in nontag mode. Asynchronous queue 0 is enabled for transmission until a frame whose descriptor has its MORE bit reset is encountered.

Transmit Asynchronous Queue 1 (NP15-0 = 04H)

This command instructs FORMAC Plus to enable asynchronous queue 1 for transmission in nontag mode. Asynchronous queue 1 is enabled for transmission until a frame whose descriptor has its MORE bit reset is encountered.

Transmit Asynchronous Queue 2 (NP15-0 = 08H)

This command instructs FORMAC Plus to enable asynchronous queue 2 for transmission in the nontag mode. Asynchronous queue 2 is enabled for transmission until a frame whose descriptor has its MORE bit reset is encountered.

Abort Current Transmit Activity (NP15-0 = 10H)

When this command is issued, if FORMAC Plus is transmitting, it aborts the transmit activity from the current queue and locks the current queue.

Reset Transmit Queues (NP15-0 = 20H)

Issuing this command in tag mode resets the internal FORMAC Plus transmit queue pointers to the start of each queue. The synchronous, asynchronous 0, asynchronous 1, and asynchronous 2 queues are reinitialized, and special-frame pointers and receive queues are unaffected. Any transmit frames that are queued when this command is issued are lost. In nontag mode this command resets all the existing transmit commands.

Set Tag Bit (NP15-0 = 30H)

When writing to buffer memory from MDRL and MDRU, this command sets the tag-bit of the next long word written. This command applies to tag mode only. It is valid for one NP write operation only.

Enable Receive Single Frame (NP15-0 = 40H)

This command is useful in tag mode only for single frame receive operation. When this command is given, FORMAC Plus enables the assertion of the RDATA signal to indicate the availability of a receive frame.

Initialization Values for Timers, Counters, and Related Registers

Table 14 lists the values of the station-address register, the MAC information register, and various timers and counters, after a hard or soft reset.

Table 14. Summary of Initialization Values for Timers, Counters and Registers.

Name	Condition After Hard or Soft Reset
Station-Address Registers	Not reset
MAC Information Registers (MIR1 and MIR0)	Both reset to 0000
TMAX register	Reset to 0000
TVX register & timer	Reset to FF00H
TREQ registers	Not reset
Priority-Sequence Registers (PRI0-2)	Each is reset to FFFFH
Token rotation timer (TRT)	Reset to 0000 and enabled
Token holding timer (THT)	Reset to FFFFH
TNEG register	Reset to 0000
TSYNC register	Reset to 0000
Frame Counter (FRMCTR)	Reset to 0000
Error Counter (ERRCTR)	Reset to 0000
Lost Counter (LSTCNTR)	Reset to 0000

FDDI Timer Implementation

Programming the timers loads the counters with their start-count value. The value programmed in the timer registers must be the two's complement of the number of 80 ns clocks. Note the following:

1. TRT and THT are implemented as 21-bit up-counters that may count from 0 to 1FFFFFH. When a timer reaches 1FFFFFH, it has expired.
2. The TVX timer is implemented as an 8-bit up counter clocked at a rate that is 1/255 of BCLK. When the TVX timer expires, it sets the STVXEXP bit in status register 2 (bit 11 in ST2L).
3. When TRT expires with a late count not equal to zero, it sets the STRTEXP bit in status register 2 (bit 10 in ST2L).

Station-Address Registers

FORMAC Plus station-addressing implements individual and group addresses as combinations of long and short addresses. These combinations are referred to as: Short Address Individual (SAID); Long Address Individual (LAID); Short Address Group (SAGP); and Long Address Group (LAGP). A short address requires 16 bits, and a long address requires 48 bits.

The 16-bit address values can be read or written via the NP bus. These registers may only be written into while in initilization mode. If a write is attempted in other modes it is ignored.

MAC Information Register (MIR)

The MIR stores the first four bytes following the source address of a MAC frame. In the case of claim frames, this field represents the T_Bid_RC value, as per the FDDI specification. When the FORMAC Plus is configured for loopback mode, the MIR stores the four bytes following the source address of any frame received. This provides a means of in-circuit testing without external hardware.

The MIR is composed of two separately addressable 16-bit read-only registers (MIR0 and MIR1). MIR1 contains the most significant word, or the first two bytes received from the media. MIR0 contains the least significant word, or the next two bytes received from the media (i.e. after the first two).

MIR is loaded sequentially with bytes as they arrive on the FORMAC Plus internal receive bus. When reading MIR1 and MIR0, it is important to realize that these registers only hold the correct value from the time the first four information bytes are received until the next frame arrives. Thus the MIR registers may only be useful for loopback testing where the frame reception is under user control, or at times when the protocol insures successive reception of frames with identical information fields.

Priority-Sequence Registers. PRI2-0

Each priority-sequence register is 16-bits long and can be written and read by the NP. These three registers set the priority levels for the corresponding asynchronous transmit queues. Upon capture of the token, and after transmission of synchronous queues, FORMAC Plus looks for queued asynchronous frames and services them in the fixed order: asynchronous queue 0, asynchronous queue 1, and asynchronous queue 2. The priority-sequence registers are used for allocating asynchronous bandwidth to each of these queues.

An asynchronous queue can be transmitted once the proper token is captured and the THT value is greater than the priority threshold value programmed into the priority register for that queue, and transmission from that queue is enabled. The contents of the priority registers are compared to the upper 16-bits of THT. After transmission of each frame the priority registers are again checked for prioritizing the transmit sequence. Transmission of asynchronous queues is continued until the queue becomes empty or the conditions for transmission are not satisfied (i.e. THT is less than the priority value for that queue). Once transmission is complete, the token is released. In nontag mode, transmission from any asynchronous queue can be enabled using the appropriate command through command register 2. In tag mode, no such command is needed since the FORMAC plus monitors the loading of transmit frames in buffer memory. Correct behavior is not guaranteed if a register value is changed during a token-holding period.

Timer and Counter Registers

TMAX Register

As per the FDDI specification, the expected token rotation time (TRT) is negotiated through the token claiming procedure. Upon initialization, reset or recovery, a default token-rotation time, designated TMAX, is loaded into TRT. The FDDI default value for TMAX is 165 ms. During the claim procedure, TMAX is used as the station's TOPR (T_Operational).

The TMAX register contains the user-specified TMAX value. TMAX is a single 16-bit register. The value of TMAX is represented as the 2's complement of the desired number of clocks between 1 and 64K (0 to FFFF). The time value associated with TMAX is a function of the BCLK frequency. The TMAX value is loaded into the upper 16 bits of the TRT timer. FDDI specifies a TMAX default value of at least 165 ms. At a clock rate of 12.5

MHz, a TMAX two's-complement value of 03C7H yields a TMAX of 165.29664 ms. In general, the TMAX register value can be determined from the following algorithm:

TMAX = Two's complement of
[(required time / 80 ns) / 32]

TVX Register and Timer (Valid-Transmission Timer)

The TVX value, is defined as the expected time between valid transmissions. Each station maintains a TVX timer that checks the time between the end delimiters of the valid frames received. Should this timer expire, a problem is assumed and the station attempts to recover the ring.

The TVX register allows the user to specify the value of the TVX counter. TVX is a single 8-bit register. The value of TVX is represented as the 2's complement of the desired number of clocks between 1 and 256 (0 to FF). The time value associated with TVX is a function of the BCLK frequency. The TVX timer is clocked at 1/255 the BCLK rate.

FDDI specifies a TVX default value of at least 2.5 ms. At a clock rate of 12.5 MHz, a TVX value of 85H translates to a 2.50 ms time value. The TVX value can be determined from the following algorithm:

TVX = Two's complement of
[(required time/80 ns)/255]

Loading TVX means writing into the TVX register. Reading TVX puts the TVX timer value on the most significant byte of the NP bus, and the previously written TVX register value on the least significant byte of the NP bus.

The TVX timer can be loaded with the value stored in the TVX register by using the NP-bus "load TVX timer from TVX register" command to command register 1. This is provided only for diagnostic purposes and is not intended for normal operation.

Requested TRT Register (TREQ)

The requested TRT value (same as TTRT, per FDDI) is stored in the TREQ register. This 32-bit value is used by the station during the claim process for comparison against the incoming claim values. Two 16-bit words are used to store the station's TREQ value. The most significant 16-bits are stored in TREQ1, and the least significant 16-bits are stored in TREQ0.

Note: The TREQ value must be the same as the T_Bid value programmed in this station's claim frame.

Token-Rotation Timer (TRT)

The token rotation timer is loaded with different values during different phases of token ring operation, as defined in the FDDI standards. When TRT expires, and the late count is greater than zero, it indicates a problem on the ring, and the ring goes into the recovery mode; i.e., it enters a claim process (T4 state in the FDDI transmit state-machine). If, however, the late count is equal to zero, ring recovery is not necessary. In this case, the late count is incremented, and TRT is reset with the latest negotiated time T_Neg (T_Opr in the FDDI standards).

The TRT can be read or written (for test purposes only) under processor control using the NP interface. The upper 16-bits of the TRT can be read directly, and the lower five bits are obtained by reading the TMRS register.

Token Holding Timer (THT)

The token holding timer is initialized with the TRT value when the token is captured and the late count is zero. THT controls the duration for which the station can transmit asynchronous frames.

The THT can be read or written (for test purposes only) under processor control using the NP interface. The upper 16-bits of the THT can be read directly, and the lower 5-bits are obtained by reading the TMRS register.

Negotiated TRT Register (TNEG)

After the claim process, the lower 21 bits of the negotiated TRT is stored in the 21-bit TNEG register. The upper 11 bits of negotiated TRT are all 1's and do not contribute to timer operation. The upper 16-bits of the TNEG register can be read directly, and the lower 5-bits are obtained by reading the TMRS register.

Synchronous-Transmission Bandwidth Register and TMSYNC Timer (TSYNC and TMSYNC)

The TSYNC register is programmed to allocate synchronous transmit bandwidth. Writing to the TSYNC register programs the upper 16 bits of a 21-bit counter that is clocked with the 80 ns BCLK. After ring recovery, upper-layer protocols negotiate for synchronous bandwidth, and the result is used to program TSYNC. Assuming that the upper-layer protocol result is an allocated time value, then the TSYNC register can be programmed by using the following algorithm:

TSYNC = Two's complement of [(allocated time / 80 ns) – maximum synchronous frame length] / 32

If frames are queued for synchronous transmission during this token period (XDONE has not been reached), and TSYNC is less than 1FFFFFH, then FORMAC Plus transmits the next synchronous frame.

A value of zero in TSYNC provides the maximum synchronous bandwidth. Synchronous-frame transmission proceeds as long as TSYNC is less than 1FFFFFH, or

XDONE in a frame descriptor is not encountered, and other conditions for transmission are satisfied.

The TMSYNC timer is loaded from the TSYNC register value at the begining of synchronous transmission and is clocked on every BCLK (80 ns).

Frame Counter. (FCNTR)

The frame counter is a 16-bit counter that counts all the frames received, as defined in FDDI standards. Overflow of the counter sets the status bit SFRMCTR in status register 2 (bit 4 of ST2L). This counter can be written with a preset value and can be read using the NP interface.

Error Counter. (ECNTR)

The error counter is a 16-bit counter that counts all error frames (as per FDDI standards) detected by this station and no other previous station. Frames received with the E Indicator set to S are not counted. Overflow of the counter sets the status bit SERRCTR in status register 2 (bit 5 of ST2L). This counter can be written with a preset value and can be read using the NP interface.

Lost Counter. (LCNTR)

The lost counter (LCNTR) is a 16-bit counter that counts all the frames/tokens being received by the FORMAC Plus that have an error (as per FDDI standards). Overflow of the counter sets the satus bit SLSTCTR in status register 2 (bit 6 of ST2L). This counter can be written with a preset value and can be read using the NP interface.

TMRS Register

The TMRS register is a read-only register that contains the lower bits of TNEG, TRT, THT timers and the late count. Bits 14–10 are the lower 5-bits of TNEG, bits 9–5 are the lower TRT bits and bits 4–0 reflect the lower THT bits. Bit 15 indicates the current state of the late count.

MAC State-Machine Register

The state machine register is a 16-bit read-only register that indicates the current states of the transmit and receive state machines as per the FDDI MAC-protocol specification. The bit assignments in this register are shown in Figure 22 and described in the following paragraphs.

Bits 0 and 1. Reserved

MDRTAG. (bit 2)

This is the tag bit of the long word read into MDRL and MDRU during the NP read operation. This applies to tag mode only.

SNPPND. (bit 3)

SNPPND, when set, indicates that an MDR request to read or write from buffer memory is pending, awaiting arbitration and service. If SNPPND is zero, the NP can issue further MDR requests. The NP typically reads this register before it issues the next request.

Transmitter State. (bits 4, 5, and 6)

Bits 4, 5, and 6 provide a 3-bit binary value for each of the transmit state-machine states, as defined in the FDDI specification. Bit 4 is the LSB and bit 6 is the MSB. **Note**: Send-immediate mode is coded as 110.

Receiver State. (bits 7, 8, and 9)

Bits 7, 8, and 9 provide a 3-bit binary value for each of the receive state-machine states, as defined in the FDDI specification. Bit 7 is the LSB and bit 9 is the MSB.

TM0 and TM1. (bits 10 and 11)

Bits 10 (TM0) and 11 (TM1) indicate the current token mode. Table 15 shows the token modes indicated by the various states of these two bits.

Table 15. Summary of TM0 and TM1 Bit Assignments for Different Token Mode.

TM0 (bit 10)	TM1 (bit 11)	Indicated Token Mode
0	0	Nonrestricted token mode.
0	1	Enter nonrestricted token mode.
1	0	Enter restricted token mode.
1	1	Restricted token mode.

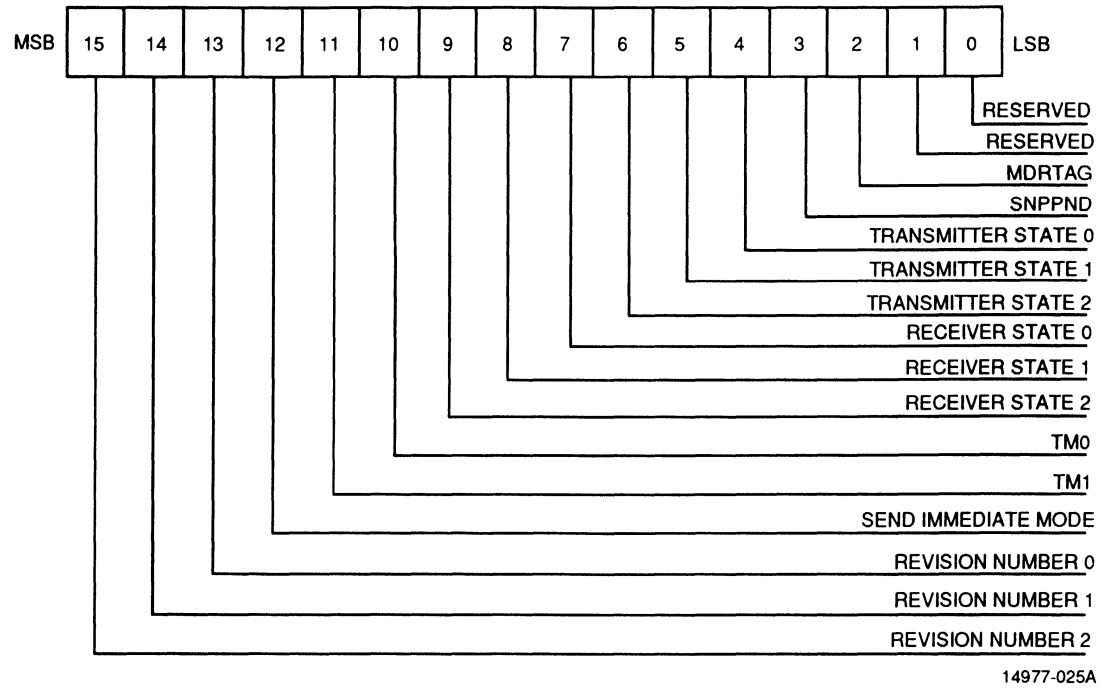


Figure 22. State Machine Register

Send Immediate Mode. (bit 12)

Bit 12, when asserted, indicates that FORMAC Plus is programmed for send-immediate mode.

Revision Number. (bits 13, 14, and 15).

Bits 13, 14, and 15 provide a three-bit binary value that indicates the revision number of the FORMAC Plus.

Programming The Buffer-Memory-Management Registers

Figure 5 shows the buffer-memory organization for both tag and nontag modes. All buffer-memory-management registers are 16 bits. The node-processor bus (NPADDR) addresses for loading or reading these registers are listed in the Table of Programmable Resources under Programming the FORMAC Plus.

Reset Status

Except for the frame threshold register, FRMTHR, which is reset to 0000, no other buffer-memory-management register is reset to a specific state.

Buffer-Memory-Management Registers In Nontag Mode

In nontag mode, the registers described in the following paragraphs are used to control access to buffer memory.

End Addresses (nontag mode)

In nontag mode, FORMAC Plus uses the value of the claim/beacon end address plus 1 (i.e. EACB+1) as the start of the receive area. The FORMAC Plus expects to see the EACB+1 value as less than the EARV value; otherwise, correct operation cannot be assured. These registers are listed as follows:

EACB: End Address of Claim/Beacon Queue

EACB+1: Start Address of Receive Queue

EARV: End Address of Receive Queue

Special-Frame Pointers (nontag mode)

The WPXSF pointer is used for loading Claim, Beacon, or Auto-Void frames in Buffer Memory. The FORMAC Plus provides the SACL register to access the Claim frame and the SABC register to access the Beacon frame. See the discussion of SACL and SABC operation under Transmitting Claim/Beacon/Auto-Void Frames (nontag mode).

While multiple Claim and Beacon frames can be stored in Buffer Memory, only one Auto-Void frame is permitted and its 16-bit pointer must be loaded at location 0000. The read pointer RPXSF is used for reading special frames for transmission. RPXSF is incremented after

every read of special frames. These registers and pointers are listed as follows:

SACL : Pointer to a Pointer to the Claim Frame

SABC : Pointer to a Pointer to the Beacon Frame

WPXSF: Write Pointer for Special Frames

RPXSF: Read pointer for Special Frames

Receive Pointers (nontag mode)

FORMAC Plus uses three pointers to receive frames into buffer memory. WPR holds the address of the next long word to be written into buffer memory. SWPR points to the first location of the current frame being written to buffer memory. The status and length of the receivced frame is loaded at this location. RPR maintains the current address for a host read of the received queue. At initialization, RPR must be equal to SWPR and WPR must be equal to SWPR+1. The three receive pointers are listed as follows:

WPR: Write Pointer for Receive Queue

SWPR: Shadow Write Pointer for Receive Queue

RPR: Read Pointer for Receive Queue

Read Transmit Pointers (nontag mode)

FORMAC Plus maintains a set of read pointers for each transmit queue to determine the current location of data for transmission. These pointers are incremented when the corresponding queue is read. These pointers are listed as follows:

RPXS: Read Pointer for Transmit Synchronous Queue

RPXA0: Read Pointer for Transmit Asynchronous Queue 0

RPXA1: Read Pointer for Transmit Asynchronous Queue 1

RPXA2: Read Pointer for Transmit Asynchronous Queue 2

Write Transmit Pointers (nontag mode)

FORMAC Plus maintains a set of write pointers for each transmit queue to determine the current location of host writes to buffer memory. The type of host request (HSREQ2-0) determines the pointer to be used. The write transmit pointers are useful only if the host interface is used for writing to the buffer memory. These write pointers are listed as follows:

WPXS: Write Pointer for Transmit Synchronous Queue

WPXA0: Write Pointer for Transmit Asynchronous Queue 0

WPXA1: Write Pointer for Transmit Asynchronous Queue 1

WPXA2: Write Pointer for Transmit Asynchronous Queue 2

Buffer-Memory Management Registers In Tag Mode

The following registers are used by FORMAC Plus to control memory access in the tag mode. The relationship of these pointers is shown in Figure 5.

Important: These registers are loaded during the initialization period and, with the exception of SACL, SABC, and WPXSF, must not be modified during normal on-line operation.

End Addresses (tag mode)

In tag mode, FORMAC Plus uses the end addresses of the various memory queues to detect wrap-around conditions. The end addresses are also used to determine the start addresses of the following queue. Therefore, the FORMAC Plus expects to see the queues organized in order of increasing address, as shown in Figure 5. The end-address registers are listed below in order of increasing address:

EACB: End Address of Claim/Beacon Area

EARV: End Address of Receive Queue

EAS: End Address of Synchronous Queue

EAA0: End Address of Asynchronous Queue 0

EAA1: End Address of Asynchronous Queue 1

EAA2: End Address of Asynchronous Queue 2

Special-Frame Pointers (tag mode)

FORMAC Plus uses individual start-address pointers to point to the beginnings of the claim and beacon frames in use. The auto-void frames have to be stored at location 0000. The WPXSF pointer is used for writing claim, beacon or auto-void frames in buffer memory. Multiple claim and beacon frames can be stored in buffer memory. The read pointer RPXSF is used for reading special frames for transmission. See the discussion of Buffer Memory operation for more details about using these pointers. These registers and pointers are listed as folows:

WPXSF: Write Pointer for Special Frames

RPXSF: Read Pointer for special Frames

SACL : Start Address of Claim Frame

SABC : Start Address of Beacon Frame

Receive Pointers (tag mode)

FORMAC Plus uses three pointers to receive frames into buffer memory. WPR addresses the next long word to be written to in buffer memory. SWPR points to the first long word in buffer memory following the last completely received frame by FORMAC Plus, and should

not be written to by the user during normal operation. RPR maintains the current address for a host read of the received queue. The three receive pointers are listed as follows:

WPR: Write Pointer for Receive Queue

SWPR: Shadow Write Pointer for Receive Queue

RPR: Read Pointer for Receive Queue

Shadow Transmit Pointers (tag mode)

In tag mode, the shadow transmit pointers point to the beginning of the next (incomplete or empty) frame stored in memory. These pointers are used to determine whether there is a frame in a given queue for transmission. These shadow pointers are not to be written by the user after initialization. Each shadow transmit pointer should be initialized to a value one greater than its corresponding transmit pointer. There is one shadow register for each transmit queue. These pointers are listed as follows:

SWPXS: Shadow Write Pointer for Transmit Synchronous Queue

SWPXA0: Shadow Write Pointer for Transmit Asynchronous Queue 0

SWPXA1: Shadow Write Pointer for Transmit Asynchronous Queue 1

SWPXA2: Shadow Write Pointer for Transmit Asynchronous Queue 2

Read Transmit Pointers (tag mode)

FORMAC Plus maintains a set of read pointers for each transmit queue to determine the current location of data for transmission. These pointers are listed as follows:

RPXS: Read Pointer for Transmit Synchronous Queue

RPXA0: Read Pointer for Transmit Asynchronous Queue 0

RPXA1: Read Pointer for Transmit Asynchronous Queue 1

RPXA2: Read Pointer for Transmit Asynchronous Queue 2

Write Transmit Pointers (tag mode)

FORMAC Plus maintains a set of write pointers for each transmit queue to determine the current location of host writes to the buffer memory. These pointers are listed as follows:

WPXS: Write Pointer for Transmit Synchronous Queue

WPXA0: Write Pointer for Transmit Asynchronous Queue 0

WPXA1: Write Pointer for Transmit Asynchronous Queue 1

WPXA2: Write Pointer for Transmit Asynchronous Queue 2

Frame Threshold Register. FRMTHR

This is a 16-bit register which holds the receive-frame (RTHR) threshold value (FRMTHR15-12), and the transmit-frame (XTHR) threshold value (FRMTHR11-0). See Figure 23. The frame threshold register must not be changed except in initialization mode. RTHR and XTHR are discussed in the following paragraphs.

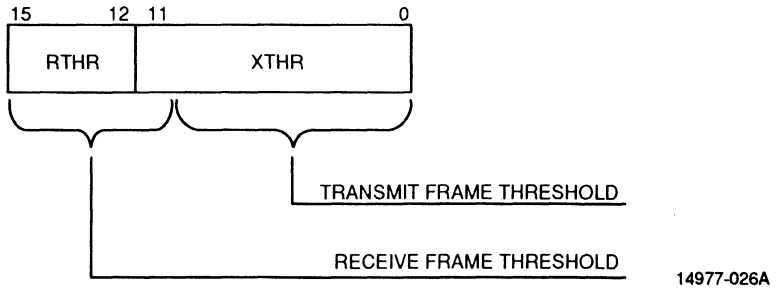


Figure 23. Frame Threshold Register

Receive Threshold. RTHR (bits 15–12 of FRMTHR)

One of the uses of this parameter is in asserting the RDATA pin in tag mode during the reception of frames, including single-frame mode.

In multi-frame mode, after the number of long words received in a frame exceeds the value of RTHR times 4, or a complete frame is received into the buffer memory, the RDATA signal is set high. A value of 0 programmed into this register disables the threshold check for setting the RDATA signal, i.e. a complete frame must be received into buffer memory before the RDATA pin is set.

In single-frame operation in tag mode the receive threshold is used differently. See the discussion of Loading Receive Frames Into Buffer Memory (Tag mode) under Buffer-Memory Operation.

Receive frame threshold is also used in the external address-detecion process in both the tag- and nontag modes. See the discussion of Special Functions under On-Line Mode.

Transmit Threshold. XTHR (bits 11–0 of FRMTHR)

XTHR is used in tag mode only. When the number of long words in the transmit queue exceeds the transmit threshold, the queue is enabled for transmission. A value of 0 programmed into this register effectively disables this function, i.e. a full frame must reside in any transmit queue before FORMAC Plus enables that queue for transmission. Availability of a full frame in buffer memory is detected through the tag bit during a host memory write.

Memory Address Register for Random Reads (MARR)

This 16-bit register is loaded by the NP with the address of the long word in the buffer memory that it wants to read through the FORMAC Plus. MARR is used during the execution of IRMEMWI and IRMEMWO instructions. In the case of an IRMEMWI instruction MARR is automatically incremented after the data is fetched in to MDRU and MDRL.

Memory Address Register for Random Writes (MARW)

This 16-bit register is loaded by the NP with the address of the long word in the buffer memory to be written through FORMAC Plus. This register is automatically incremented when MDR is written into buffer memory.

Memory Data Register for Random Access (MDR)

The memory data register (MDR) is a 32-bit register which has access to the node processor's NP-bus as well as to the buffer memory's 32-bit BD bus. Loading or reading of the MDR register from the NP bus is accomplished by separately accessing each of its two halves, i.e. MDRU (upper 16-bits), and MDRL (lower 16-bits). The MDR can be loaded from the buffer memory by the instruction IRMEMWO or IRMEMWI.

After the MDR is loaded by the NP from the NP bus, each long word is transferred into buffer memory at the location pointed to by the value in the address register (MARW). The long word address in the buffer memory for reading and writing operations is obtained from the MARR and MARW respectively. Hence, it is imperative that the appropriate address register be loaded before any of these operations is performed.

In tag mode, while performing NP writes through MDRL and MDRU, the tag bit can be set in buffer memory by using the command-register-2 30H instruction (set tag bit). See the discussion of command registers 1 and 2 under Programming the FORMAC Plus.

LOADING DATA INTO BUFFER MEMORY. To load data into buffer memory, using the MDR, proceed as follows:

1. Load the MARW with the 16-bit address of the long word in buffer memory to be written.
2. Write each half of the long word to be transferred into MRDU and MDRL. A buffer-memory write cycle will take place after both parts of the MDR are loaded.
3. Subsequent consecutive words can be loaded into buffer memory simply by writing to the MDR, since the address in MARW is automatically incremented after each buffer-memory write cycle.

READING A DATA WORD FROM BUFFER MEMORY. To read a data word from buffer memory to the node processor, using the MDR, proceed as follows:

1. Load the MARR with the 16-bit address of the long word in buffer memory to be read.
2. Issue the IRMEMWO instruction to command register 1, and then read the contents of MDRU and MDRL to the NP.

READING CONSECUTIVE WORDS FROM BUFFER MEMORY. To read a sequence of consecutive words from buffer memory to the node processor, using the MDR, proceed as follows:

1. Load the MARR with the beginning buffer-memory address of the desired sequence of long words.
2. Issue the IRMEMWI instruction to command register 1 and read the sequence of words from MDRU and MDRL to the NP.
3. To terminate the sequence of reads so that it can be resumed without having to reload MARR, first issue the IRMEMWI instruction to command register 1, and read all but the last word of the sequence to the NP through the MDR.
4. Then, issue the IRMEMWO instruction to command register 1 before reading the last word in the sequence. Because IRMEMWO does not increment MARR, the sequence can be resumed from its stopping point.

SPECIFICATIONS
FORMAC Plus FUNCTIONAL TIMINGS

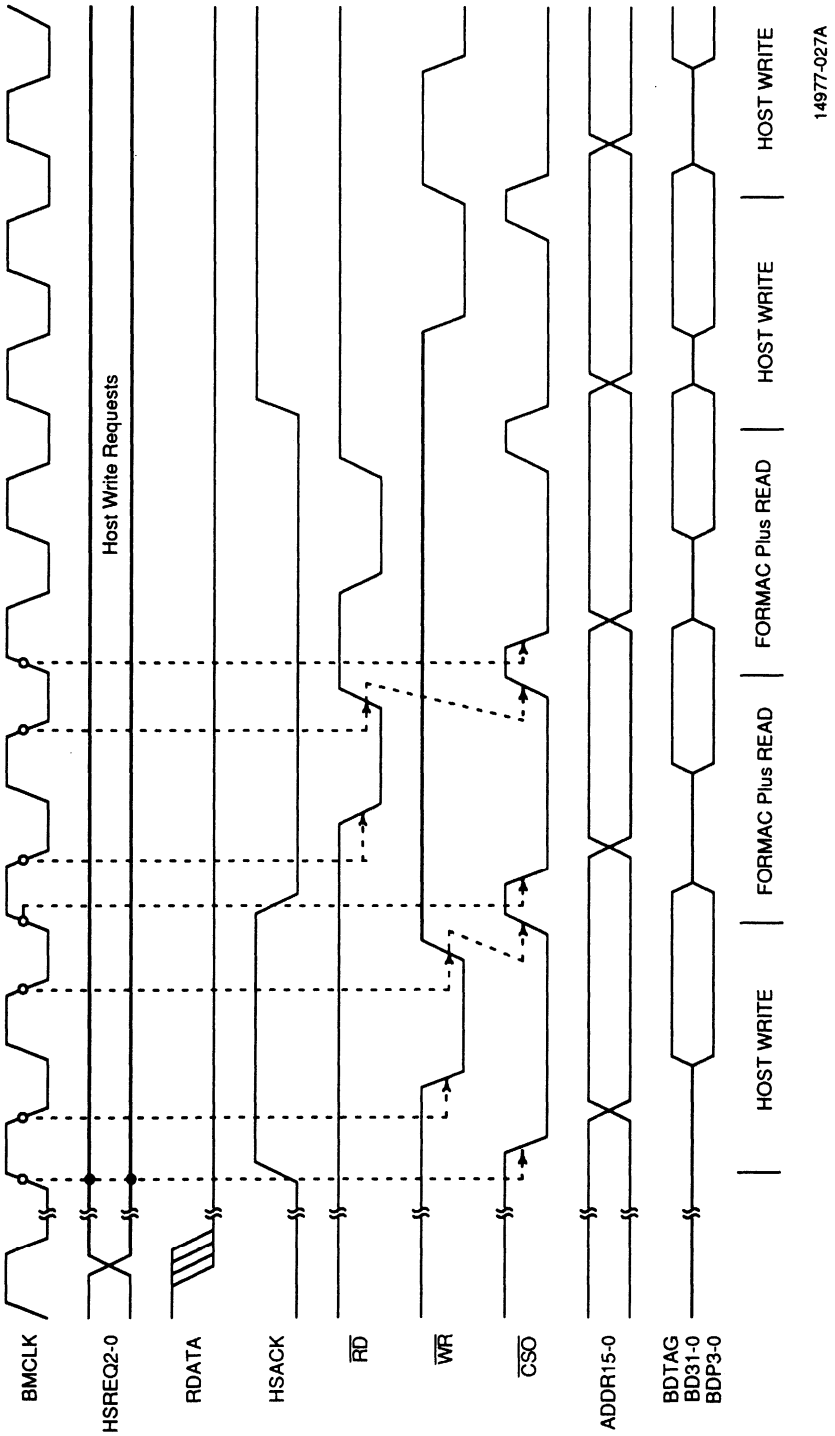


Figure 24. Host and FORMAC Plus Buffer Memory Access (Back-to-Back Read)

FORMAC Plus FUNCTIONAL TIMINGS

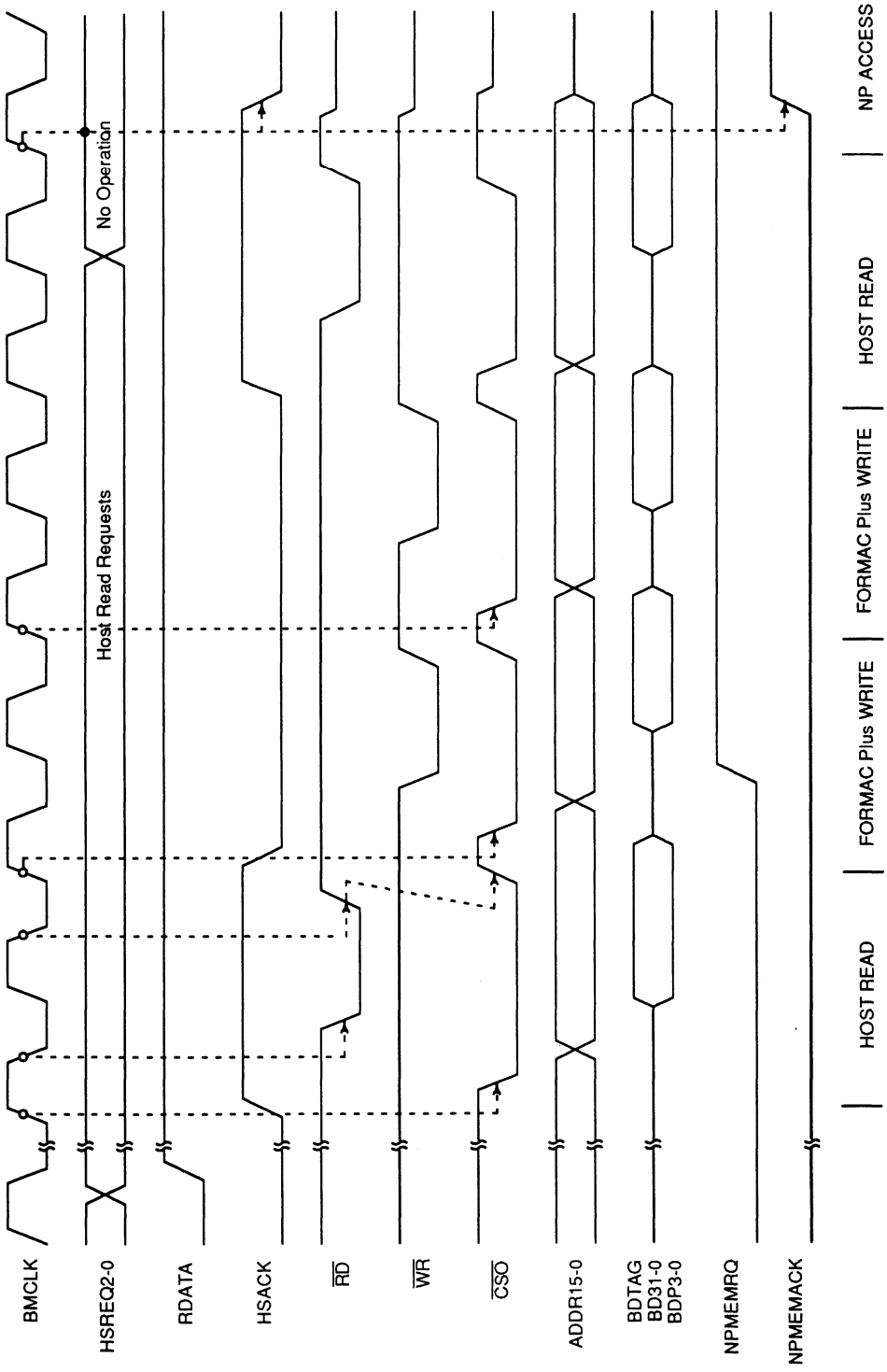


Figure 25. Host and FORMAC Plus Buffer Memory Access (Back-to-Back Write)

FORMAC Plus FUNCTIONAL TIMINGS

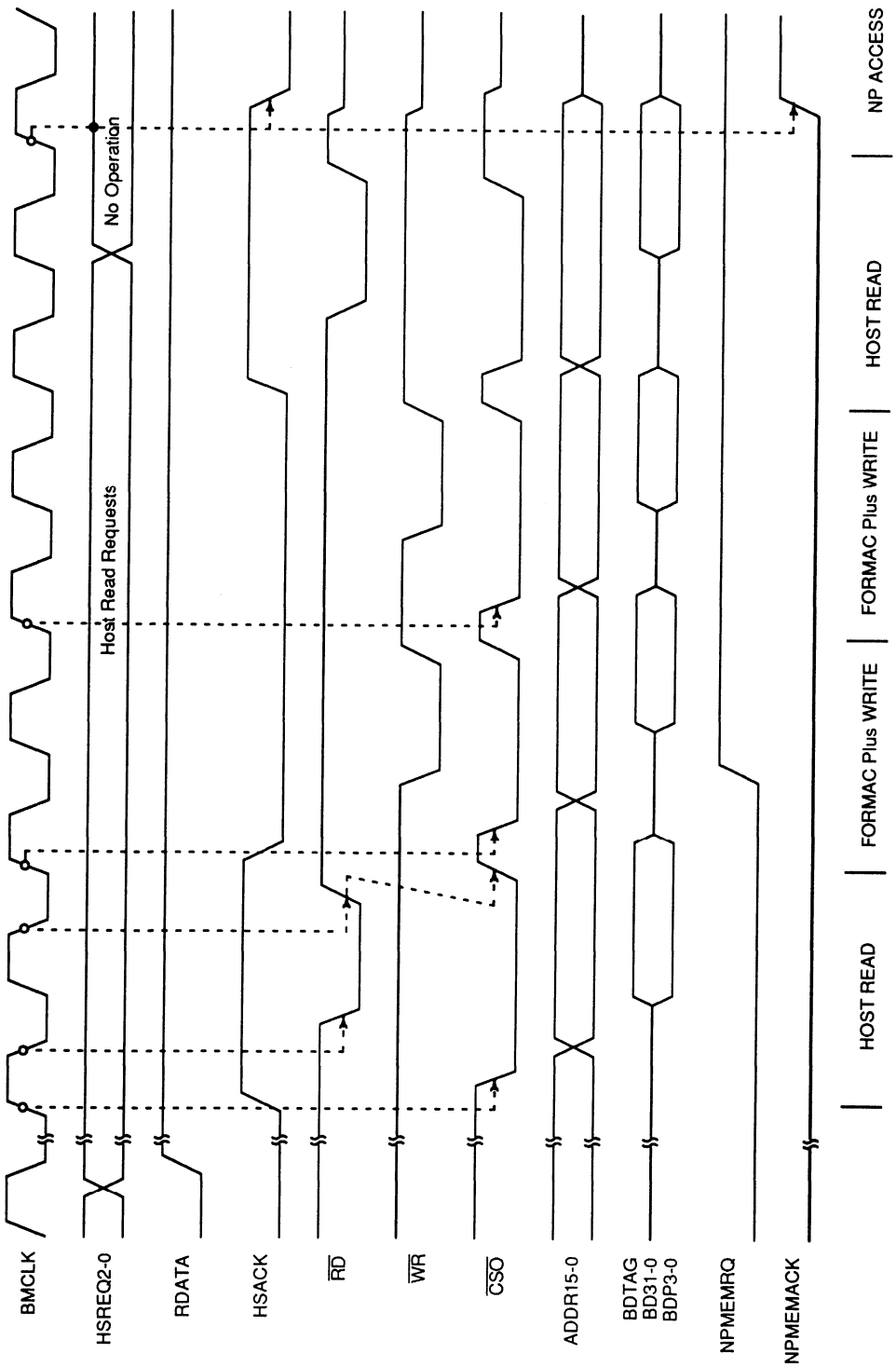
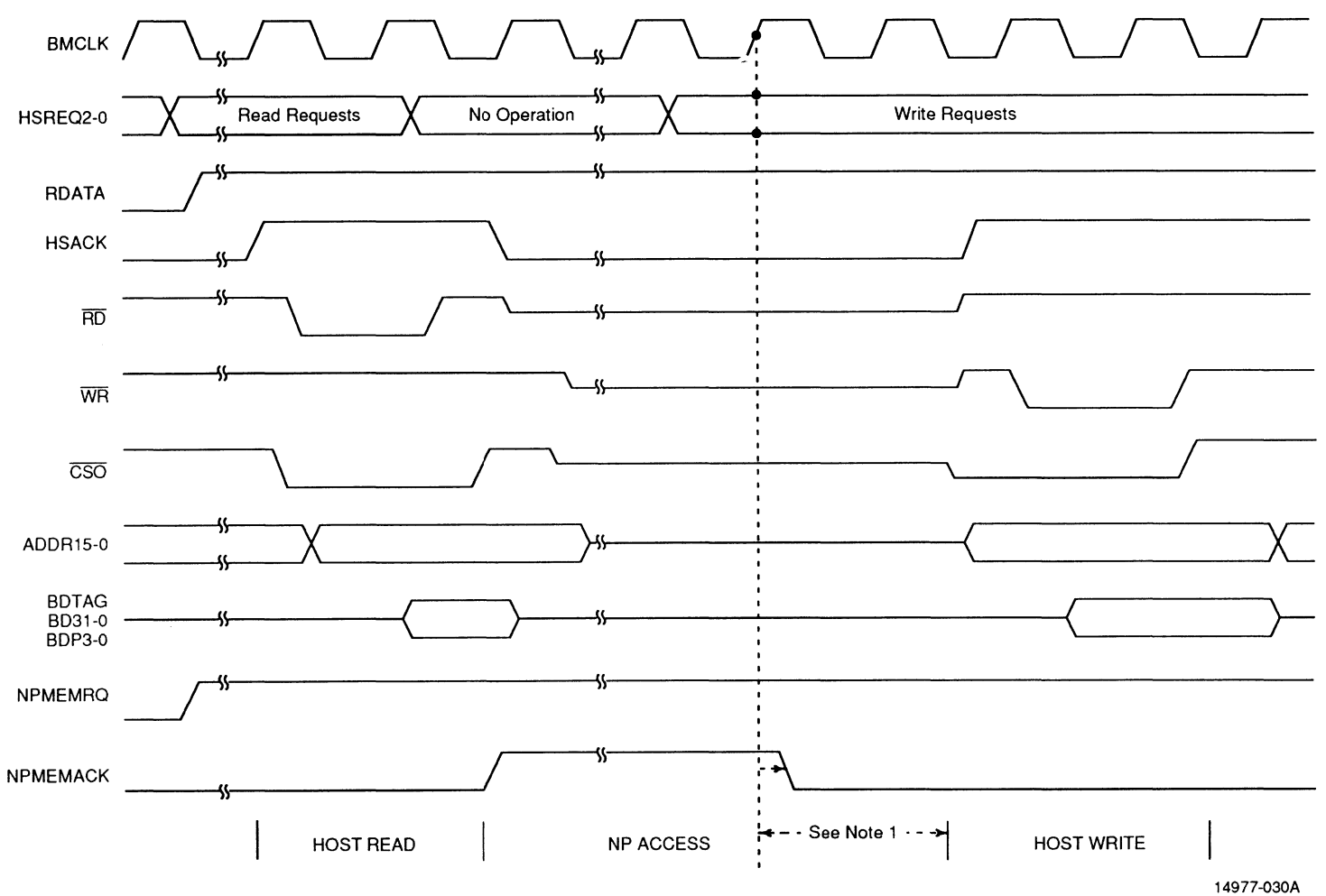


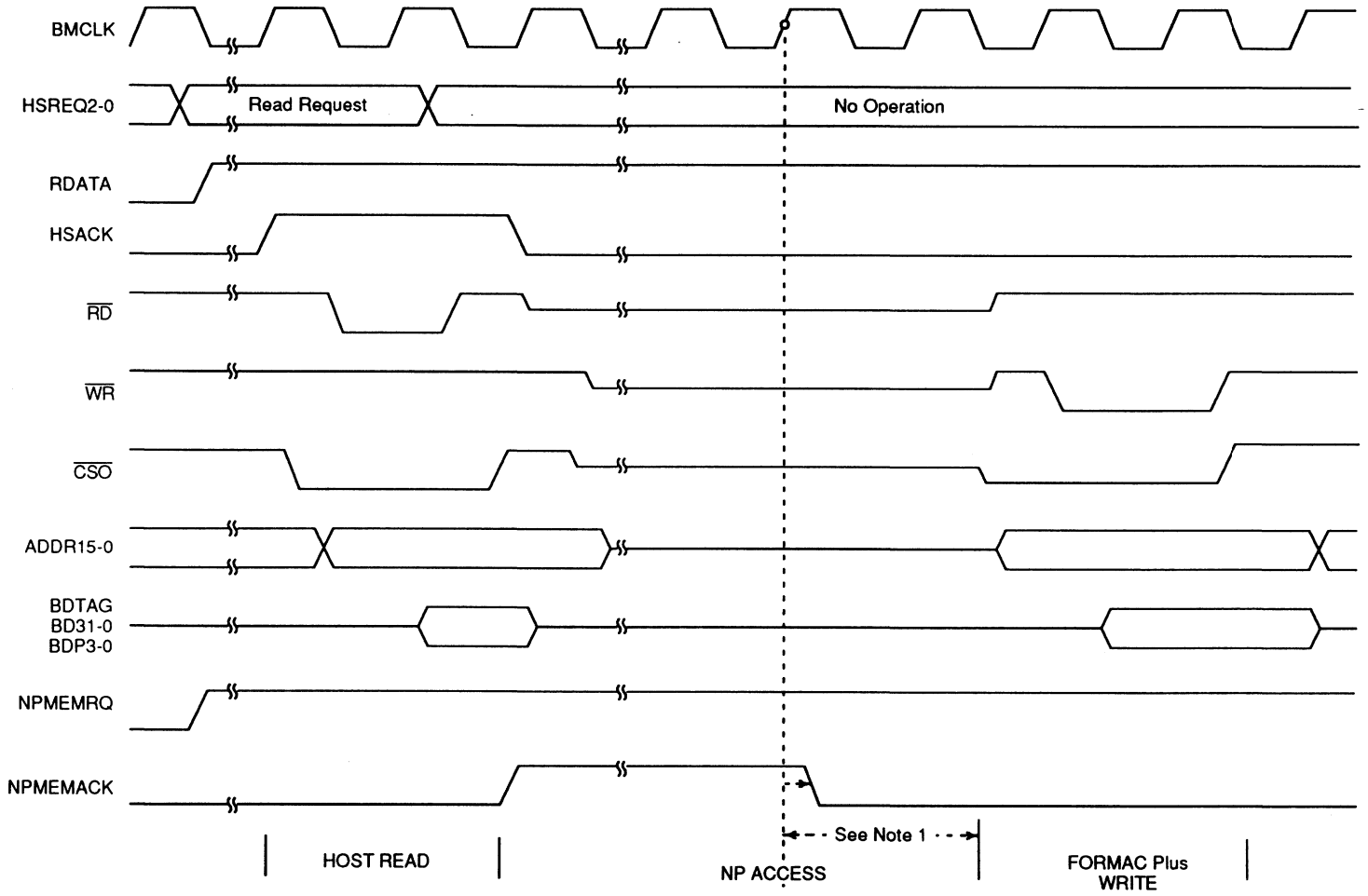
Figure 26. NP (DMA) Buffer Memory Access—Normal Handshake



Note:

1. The NP has to release the bus within 2 BMCLK periods after NPMEMACK is driven low due to a host request.

Figure 27. NP (DMA) Buffer Memory Access—Preemptive Host Write



Note:

1. The NP has to release the bus within 2 BMCLK periods after NPMEMACK is driven low due to a FORMAC Plus request.

Figure 28. NP (DMA) Buffer Memory Access—Preemptive FORMAC Plus Write

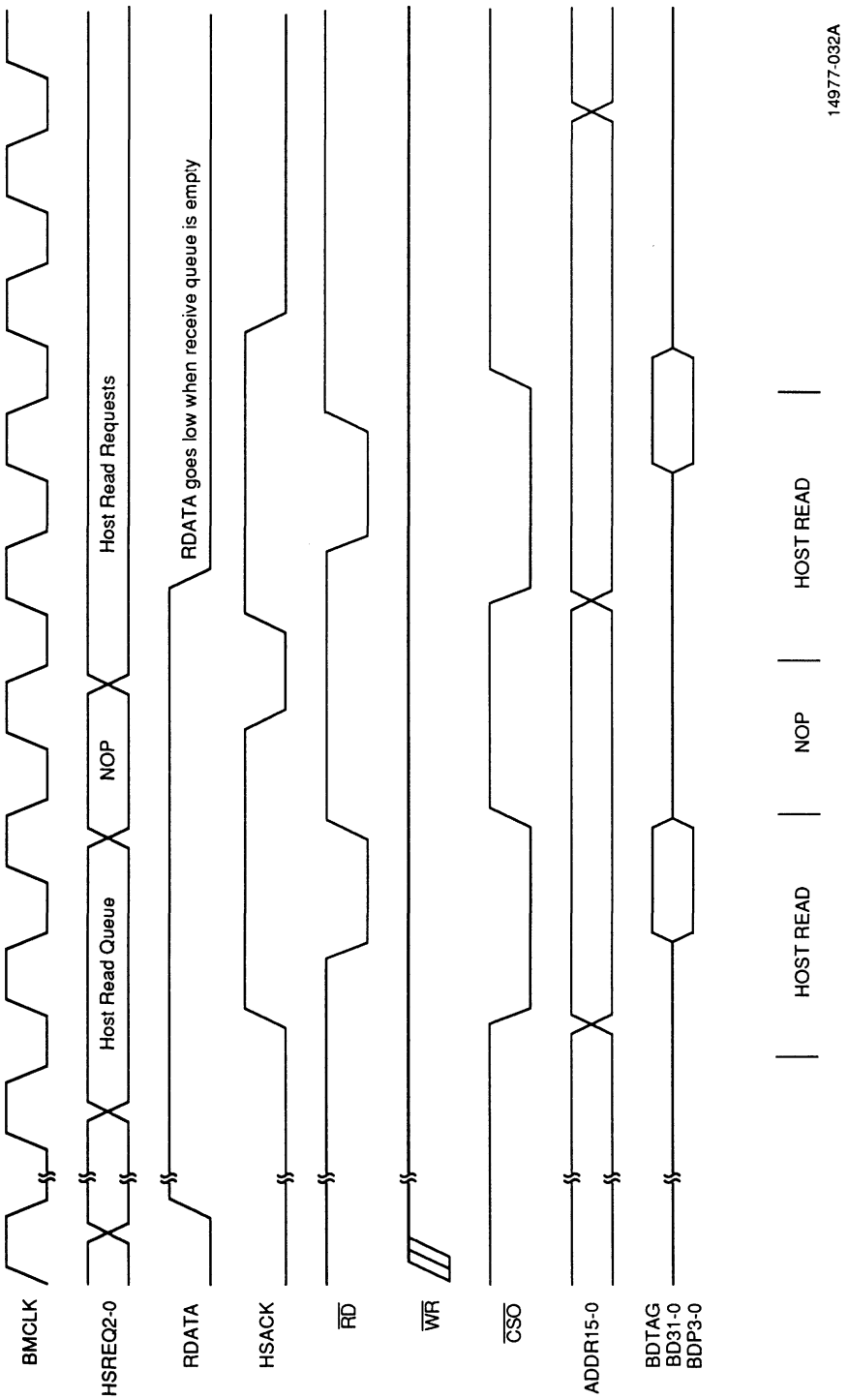


Figure 29. Host Read Receive Queue

FORMAC Plus FUNCTIONAL TIMINGS

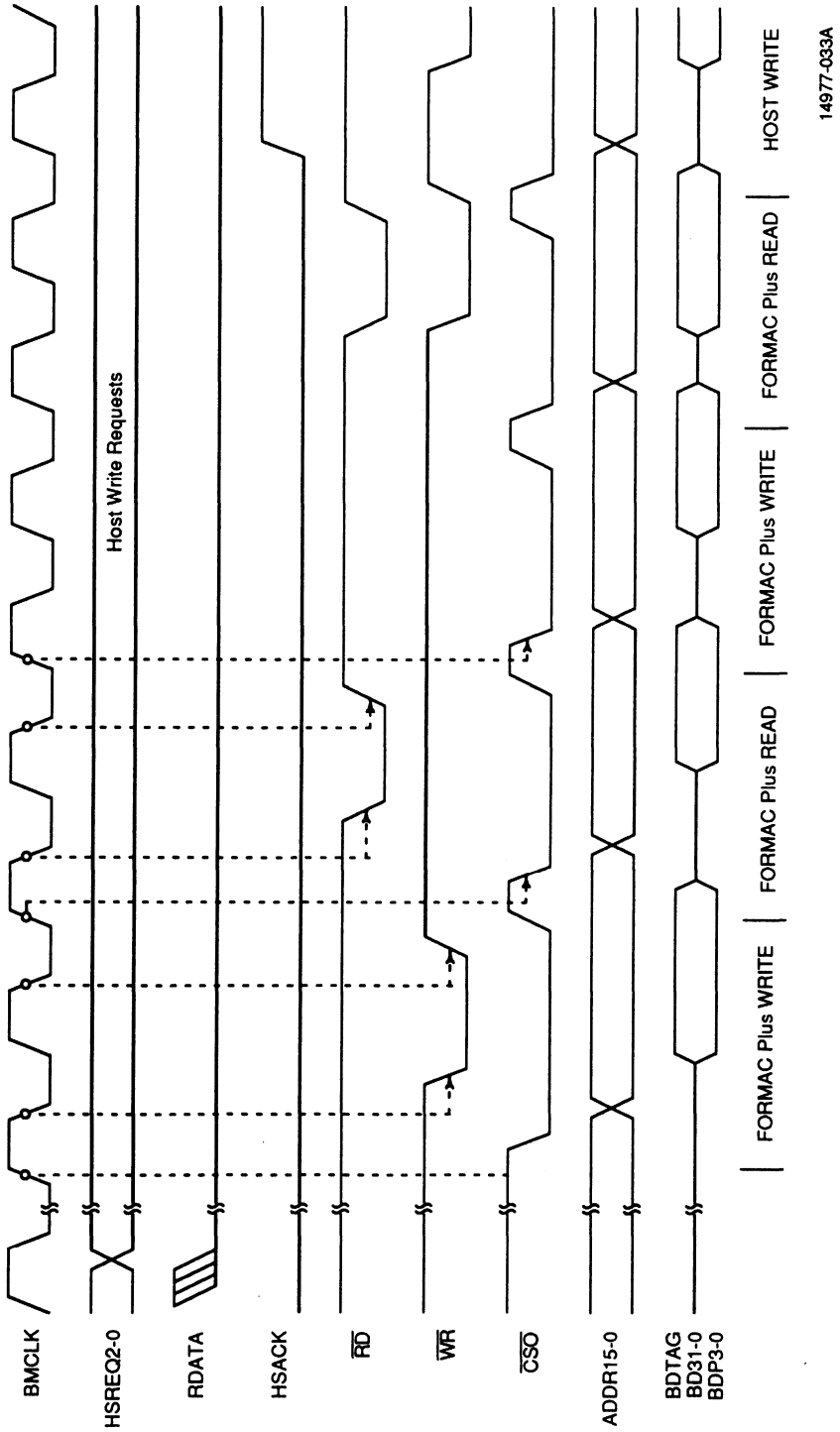


Figure 30. FORMAC Plus Buffer Memory Access

FORMAC Plus FUNCTIONAL TIMINGS

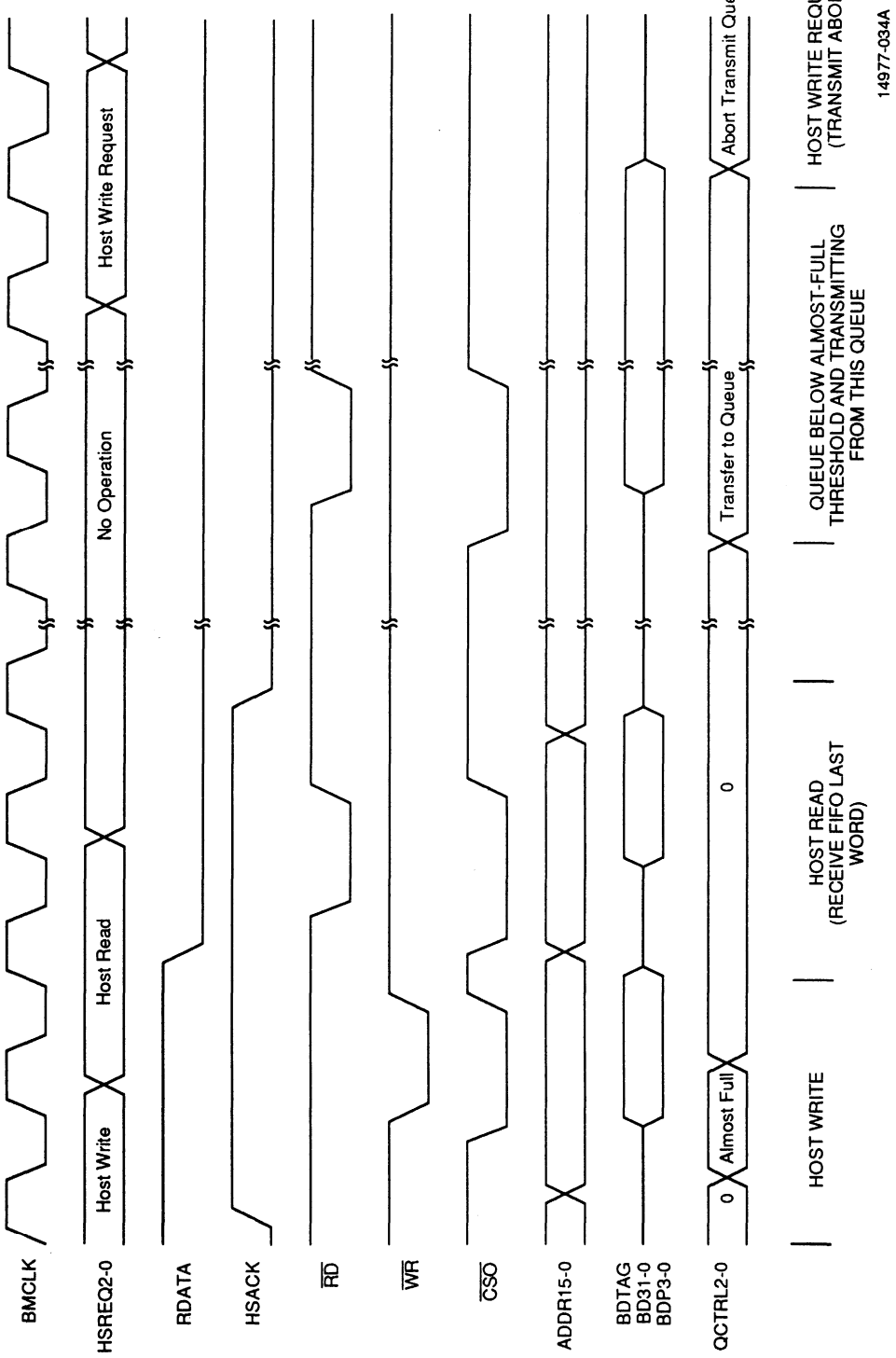
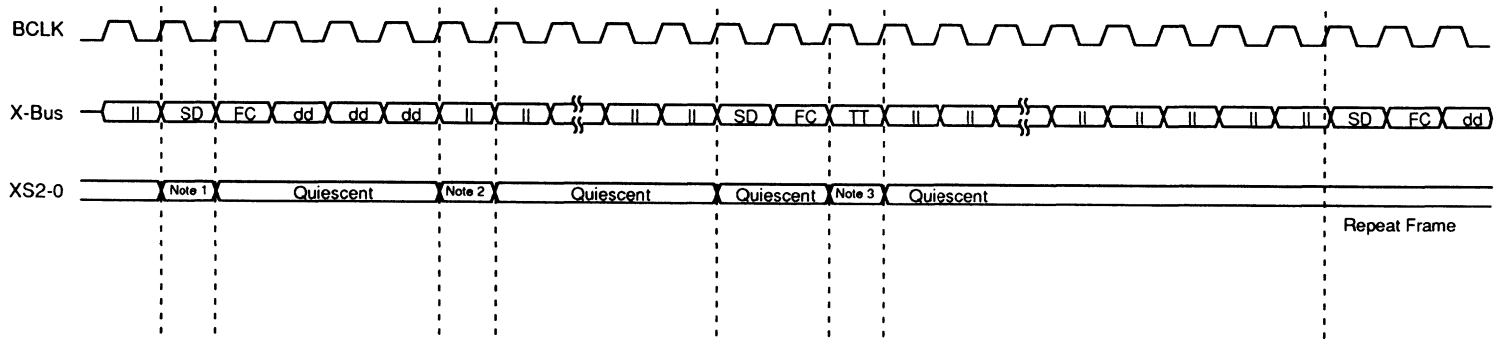


Figure 31. QCTRL and RDATA Operation During Host Buffer Memory Access



Notes:

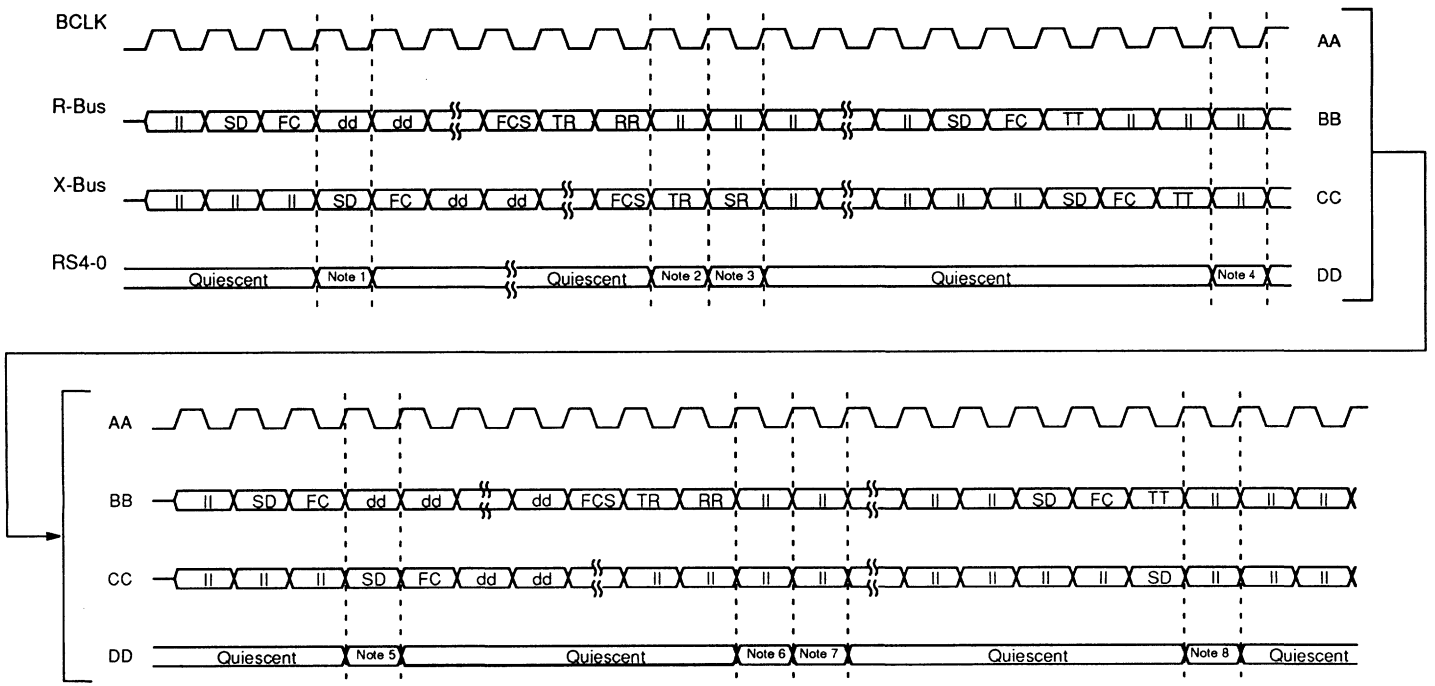
1. Transmitting Queue (Synchronous, Asynchronous 0, Asynchronous 1, and Asynchronous 2)
2. Transmit Aborted
3. Token Issued

I = Idle

dd = data bits

14977-035A

Figure 32. Timing of Transmit Status Signals



Notes:

1. Received SD of Short-address or long-address frame
2. Frame Type: Claim, Beacon Void, LLC, SMT or Implementor frame
3. Missed frame
4. Pass token: nonrestricted or restricted
5. Received SD of Short-address or long-address frame
6. Frame Type
7. FS Valid and E, A, C, indicators are received
8. Capture Token: nonrestricted or restricted

dd = data bits

I = Idle symbol

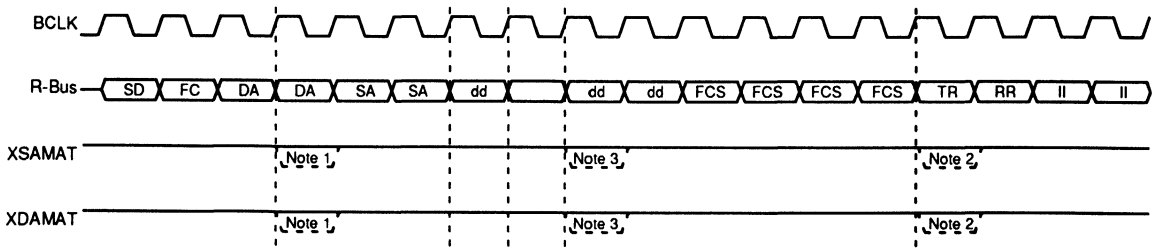
S = Set

R = Reset

14977-036A

Figure 33. Receive Status Signals Timing

FORMAC Plus FUNCTIONAL TIMINGS



Notes:

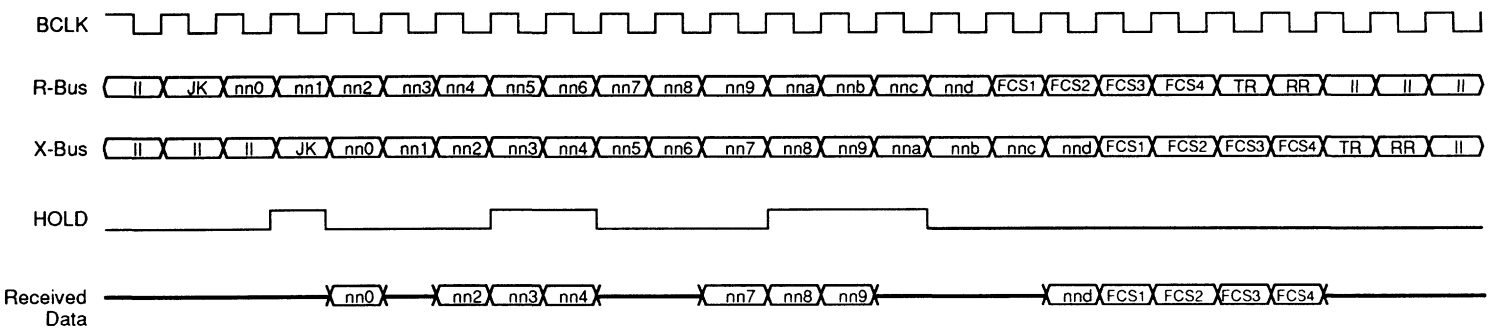
1. Earliest allowed assertion
2. Latest allowed assertion if RTHR = 0 or receive threshold not crossed
3. Latest allowed assertion if RTHR ≠ 0 (before receive threshold crossed)—based on RTHR value programmed

dd = data bits

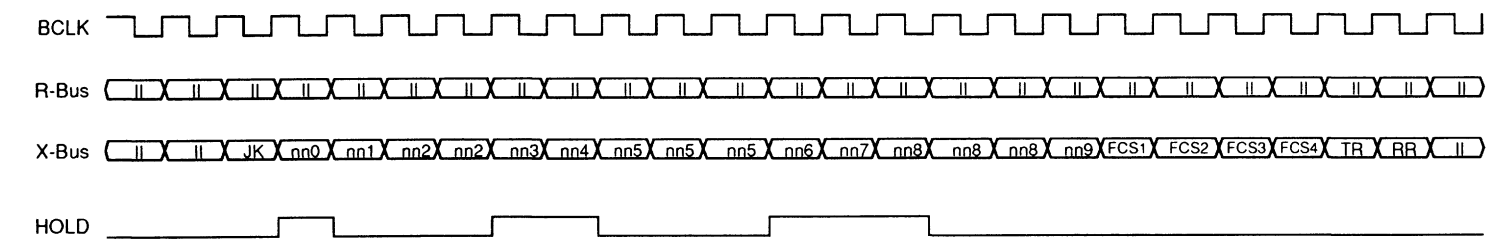
I = Idle symbol

14977-037A

Figure 34. External Address Detection



Receive Hold Timings



Transmit Hold Timings

Notes:

nn = data
I = idle
T = End Delimiter in a Frame
JK = Start Delimiter in a Frame
FCS = Frame Check Sequence

14977-038A

Figure 35. Hold Operation

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature	0 to 70°C
Supply Voltage Referenced to V_{SS}	−0.3 to +6 V
DC Voltage applied to any Pin Referenced to V_{SS}	−0.5 to V_{DD} + 0.5 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Temperature, T_A	0°C to 70°C
Supply Voltage, V_{CC}	4.75 V to 5.25 V

DC CHARACTERISTICS over COMMERCIAL operating ranges

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = Max.		0.4	V
V_{OH}	Output High Voltage (Note 1)	$I_{OH} = -I_{OL}/2$ mA	2.4		V
I_{OL}	Output Low Current (Note 2)			8.0	mA
I_{OL}	Output Low Current (Note 3)			4.0	mA
I_{OH}	Output High Current			$-I_{OL}/2$	mA
I_{OZ}	Output Leakage Current (Note 4)	0.4 V < V_{OUT} < V_{CC}	−10	10	µA
I_{IX}	Input Leakage Current (Note 5)	0 V < V_{IN} < V_{CC}	−10	10	µA
I_{CC}	Power Supply Current	V_{CC} = Max. f(BCLK) = 12.5 MHz f(BMCLK) = 25 MHz		175	mA

Notes:

1. V_{OH} does not apply to open-drain pins.
2. An I_{OL} value of 8.0 mA applies to the following signals : ADDR15-0, $\overline{WR}$, $\overline{RD}$, BD31-0, BDP3-0, BDTAG, $\overline{CSO}$, $\overline{MINTR1}$, $\overline{MINTR2}$, and $\overline{READY}$. Note that $\overline{MINTR1}$, $\overline{MINTR2}$ and $\overline{READY}$ are open-drain pins.
3. An I_{OL} value of 4.0 mA applies to all FORMAC Plus signals except those specified in Note 2.
4. I_{OZ} applies to all three-state output pins and bidirectional pins.
5. I_{IX} applies to all input-only pins.

CAPACITANCE (See Note 6)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
C_{IN}	Input pins			10	pF
$C_{I/O}$	Bidirectional pins (Note 7)			10	pF

Notes:

6. Pin capacitance is characterized at a frequency of 1 MHz, but is not 100% tested.
7. The following bidirectional or output pins are designed to drive a 100 pF capacitive load: BD31-0, BDTAG, BDP3-0, ADDR15-0, $\overline{CSO}$, $\overline{RD}$, $\overline{WR}$, $\overline{READY}$, $\overline{MINTR1}$, and $\overline{MINTR2}$. All other FORMAC Plus pins are designed to drive a 50 pF capacitive load.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges

Parameter No.*	Parameter Description	Min.	Max.
1	BCLK Period	80 ns	
2	BCLK HIGH Pulse Width	35 ns	
3	BCLK LOW Pulse Width	35 ns	
4	Unused		
5	$\overline{CSI}$, $\overline{DS}$ Setup Time to BCLK HIGH (Synchronous NP-Bus)	30 ns	
6	$\overline{CSI}$, $\overline{DS}$ Hold Time from BCLK HIGH (Synchronous NP-Bus)	0 ns	
7	NPADDR6-0, R/$\overline{W}$ Setup Time to BCLK HIGH	30 ns	
8	NPADDR6-0, R/$\overline{W}$ Hold time from BCLK HIGH	0 ns	
9	Unused		
10	BCLK HIGH to NPDATA15-0 Enabled	0 ns	
11	BCLK HIGH to NPDATA15-0 Valid		55 ns
12	NPDATA15-0 Hold Time from BCLK HIGH	0 ns	
13	NPDATA15-0 Disabled from BCLK HIGH		30 ns
14–16	Unused		
17	BCLK HIGH to $\overline{READY}$ LOW		20 ns
18	BCLK HIGH to $\overline{READY}$ Deasserted		30 ns
19	Unused		
20	NPDATA15-0 Write Setup Time to BCLK HIGH	20 ns	
21	NPDATA15-0 Write Hold Time from BCLK HIGH	0 ns	
22–23	Unused		
24	$\overline{DS}$ HIGH to $\overline{DS}$ LOW (Asynchronous Read/Write Recovery Time)	100 ns	
25[1]	$\overline{R/W}$ & NPADDR6-0 Setup Time to $\overline{DS}$ ($\overline{CSI}$) LOW	0 ns	
26[2]	$\overline{R/W}$ & NPADDR6-0 Hold Time from $\overline{DS}$ ($\overline{CSI}$) HIGH	0 ns	
27	Unused		
28[1]	$\overline{DS}$ ($\overline{CSI}$) LOW to NPDATA15-0 Enabled (Asynchronous Read)	0 ns	
29[1]	$\overline{DS}$ ($\overline{CSI}$) LOW to NPDATA15-0 Valid (Asynchronous Read)		235 ns
30[2]	NPDATA15-0 Hold Time from $\overline{DS}$ ($\overline{CSI}$) HIGH (Asynchronous Read)	5 ns	
31[2]	$\overline{DS}$ ($\overline{CSI}$) HIGH to NPDATA15-0 Disabled		30 ns
32	Unused		
33[1,3]	$\overline{DS}$ ($\overline{CSI}$) LOW to $\overline{READY}$ LOW		270 ns
34[2]	$\overline{DS}$ ($\overline{CSI}$) HIGH to $\overline{READY}$ Deasserted		35 ns
35	NPDATA15-0 Valid before $\overline{READY}$ LOW (Asynchronous Read)	15 ns	
36	Unused		
37[1]	NPDATA15-0 Setup Time to $\overline{DS}$ ($\overline{CSI}$) LOW (Asynchronous Write)	–60 ns	

Notes:
1. Parameter measured from $\overline{CSI}$ or $\overline{DS}$ whichever goes LOW last.
2. Parameter measured from $\overline{CSI}$ or $\overline{DS}$ whichever goes HIGH first.
3. Except for buffery memory read using MDR.

*The numbers in this column refer to the corresponding circled timing values in Figures 36 through 45.

SWITCHING CHARACTERISTICS (Continued)

Parameter No.*	Parameter Description	Min.	Max.
38[2]	NPDATA15-0 Hold Time from $\overline{DS}$ ($\overline{CSI}$) HIGH (Asynchronous Write)	0 ns	
39–43	Unused		
44	BCLK HIGH to X Bus (X0 – X7, XCU, XCL) Valid		35 ns
45	X Bus (X0 – X7, XCU, XCL) Hold Time from BCLK HIGH	6 ns	
46–47	Unused		
48	RA0 – RA7, RACU, RACL Setup Time to BCLK HIGH RB0 – RB7, RBCU, RBCL Setup Time to BCLK HIGH	10 ns	
49	RA0 – RA7, RACU, RACL Hold Time from BCLK HIGH RB0 – RB7, RBCU, RBCL Hold Time from BCLK HIGH	3 ns	
50–57	Unused		
58	BMCLK Period	40 ns	80 ns
59	BMCLK HIGH Pulse Width	45% of BMCLK	55% of BMCLK
60	BMCLK LOW Pulse Width	45% of BMCLK	55% of BMCLK
61	HSREQ2-0 Setup Time to BMCLK HIGH	20 ns	
62	HSREQ2-0 Hold Time from BMCLK HIGH	10 ns	
63	Unused		
64	BMCLK HIGH to HSACK HIGH		25 ns
65	BMCLK HIGH to HSACK LOW		25 ns
66–69	Unused		
70	BMCLK HIGH to RDATA HIGH		25 ns
71	BMCLK HIGH to RDATA LOW		25 ns
72	BMCLK HIGH to QCTRL2-0 Valid		25 ns
73	QCTRL2–0 Hold Time from BCLK HIGH	5 ns	
74	Unused		
75	NPMEMRQ Setup Time to BMCLK HIGH	15 ns	
76	NPMEMRQ Hold Time from BMCLK HIGH	10 ns	
77	BMCLK HIGH to NPMEMACK HIGH		20 ns
78	BMCLK HIGH to NPMEMACK LOW		20 ns
79–90	Unused		
91	BMCLK HIGH to ADDR15-0 Enabled	0 ns	
92	BMCLK HIGH to ADDR15-0 Valid		26 ns
93	ADDR15-0 Hold Time from $\overline{RD}$ or $\overline{WR}$ HIGH	0 ns	
94	BMCLK HIGH to ADDR15-0 Disabled		30 ns
95	BMCLK HIGH to $\overline{CSO}$ LOW		26 ns

Notes:

1. Parameter measured from $\overline{CSI}$ or $\overline{DS}$ whichever goes LOW last.
2. Parameter measured from $\overline{CSI}$ or $\overline{DS}$ whichever goes HIGH first.

*The numbers in this column refer to the corresponding circled timing values in Figures 36 through 45.

SWITCHING CHARACTERISTICS (Continued)

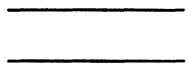
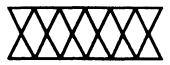
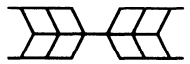
Parameter No.*	Parameter Description	Min.	Max.
96	$\overline{CSO}$ HOLD Time from $\overline{RD}$ or $\overline{WR}$ HIGH	0 ns	
97	BMCLK HIGH to $\overline{CSO}$ Disabled		30 ns
98	Unused		
99	BMCLK LOW to $\overline{RD}$ LOW		18 ns
100	BMCLK LOW to $\overline{RD}$ HIGH	8 ns	18 ns
101	BMCLK HIGH to $\overline{RD}$ Disabled		30 ns
102	Unused		
103	BD31-0, BDP3-0, BDTAG Setup Time to $\overline{RD}$ HIGH	12 ns	
104	BD31-0, BDP3-0, BDTAG Hold Time from $\overline{RD}$ HIGH	0 ns	
105	ADDR15-0 Valid to $\overline{WR}$ LOW	Note 3	
106	BMCLK LOW to $\overline{WR}$ LOW	8 ns	18 ns
107	BMCLK LOW to $\overline{WR}$ HIGH	6 ns	18 ns
108	BMCLK HIGH to $\overline{WR}$ Disabled		30 ns
109	Unused		
110	BMCLK LOW to BD31-0, BDP3-0, BDTAG Enabled	0 ns	
111	BMCLK LOW to BD31-0, BDP3-0, BDTAG Valid		26 ns
112	BD31-0, BDP3-0, BDTAG Hold Time from $\overline{WR}$ HIGH	0 ns	
113	BMCLK HIGH to BD31-0, BDP3-0, BDTAG Disabled		30 ns
114	BD31-0, BDP3-0, BDTAG Valid before $\overline{WR}$ HIGH	15 ns	
115–119	Unused		
120	BCLK HIGH to $\overline{MINTR1}$ or $\overline{MINTR2}$ LOW		25 ns
121	BCLK HIGH to $\overline{MINTR1}$ or $\overline{MINTR2}$ Deasserted		25 ns
122	Unused		
123	Hold/XMTINH Setup Time to BCLK HIGH	30 ns	
124	Hold/XMTINH Hold Time from BCLK HIGH	5 ns	
125	Unused		
126	BCLK HIGH to RS4-0, XS2-0 Valid		35 ns
127	RS4-0, XS2-0 Hold Time from BMCLK HIGH	5 ns	
128	Unused		
129	$\overline{XSAMAT}$, $\overline{XDAMAT}$ Setup Time to BCLK HIGH	20 ns	
130	$\overline{XSAMAT}$, $\overline{XDAMAT}$ Hold Time from BCLK HIGH	5 ns	
131	Unused		
132	$\overline{RESET}$ LOW Pulse Width	320 ns	

Notes:

1. Parameter measured from $\overline{CSI}$ or $\overline{DS}$ whichever goes LOW last.
2. Parameter measured from $\overline{CSI}$ or $\overline{DS}$ whichever goes HIGH first.
3. The minimum value of parameter #105 is:
   Parameter #105 (ADDR valid to $\overline{WR}$ valid) = Parameter #59 (MIN) + Parameter #106 (MIN) – Parameter #92 (MAX).

*The numbers in this column refer to the corresponding circled timing values in Figures 36 through 45.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS

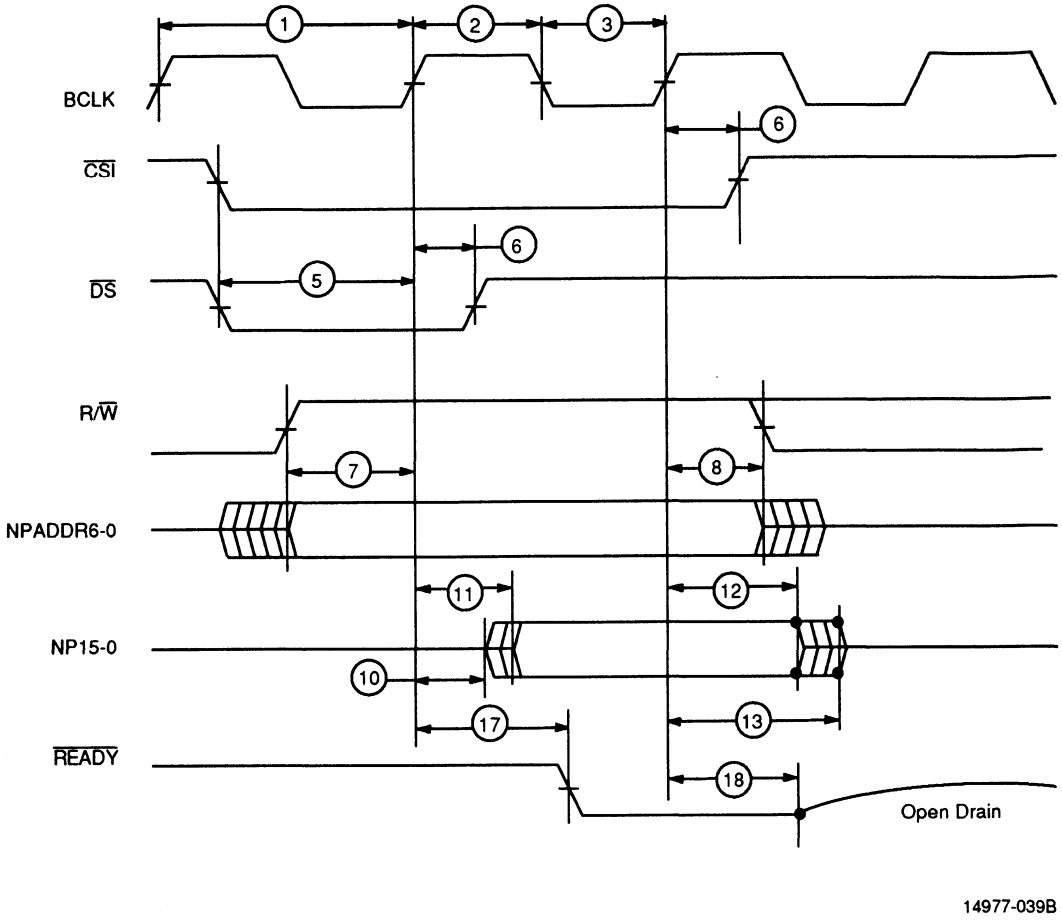


Figure 36. NP-Bus Synchronous Read Timings

SWITCHING WAVEFORMS

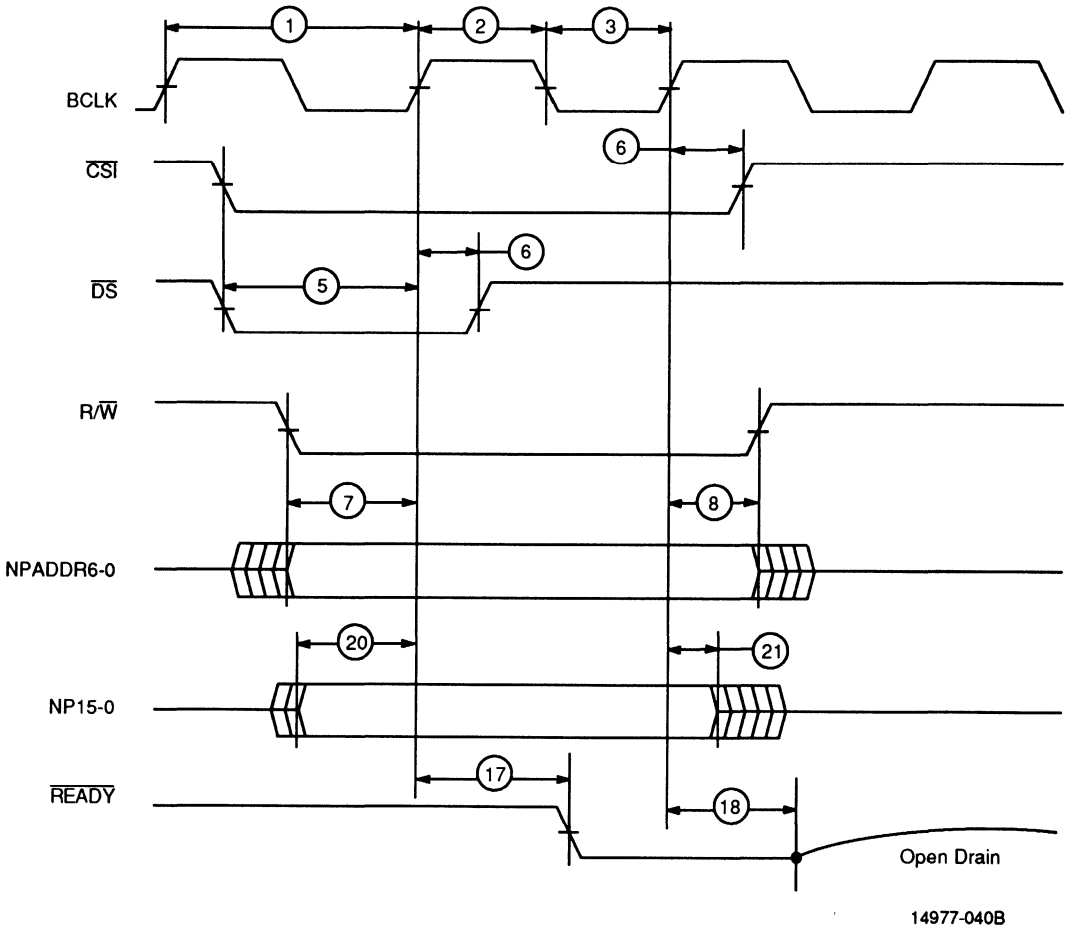
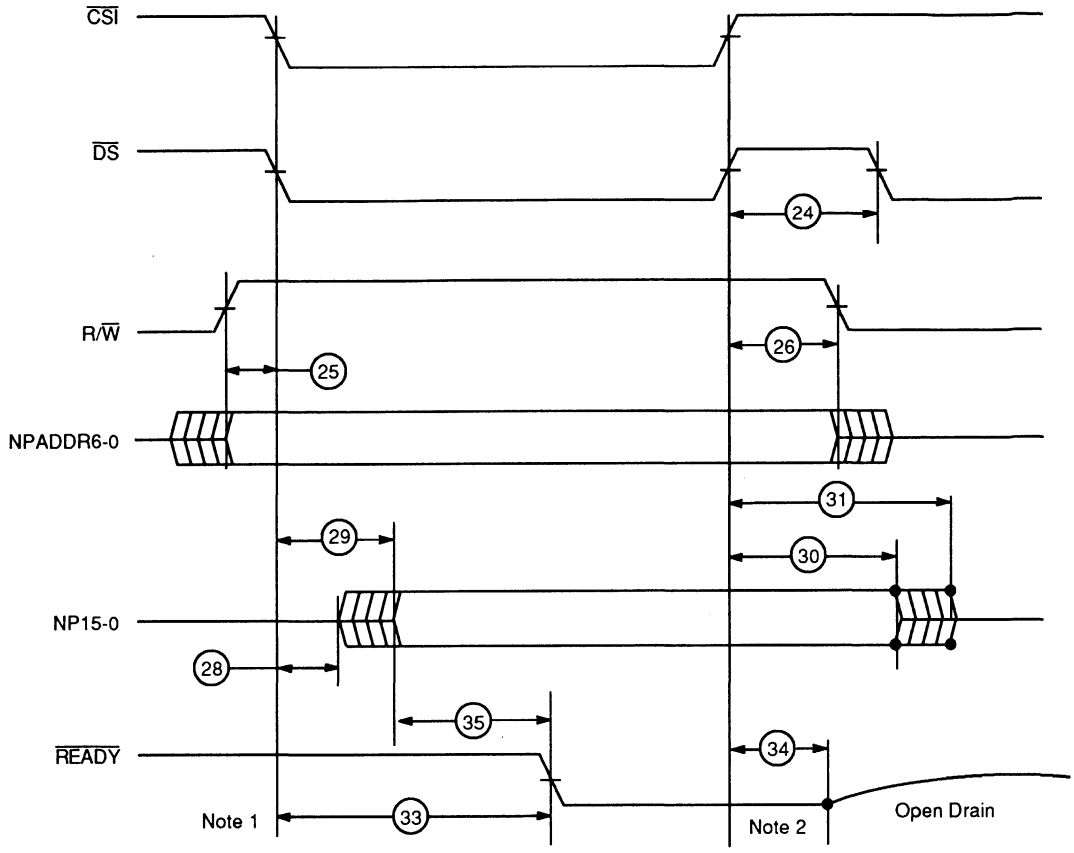


Figure 37. NP Bus Synchronous Write Timings

SWITCHING WAVEFORMS



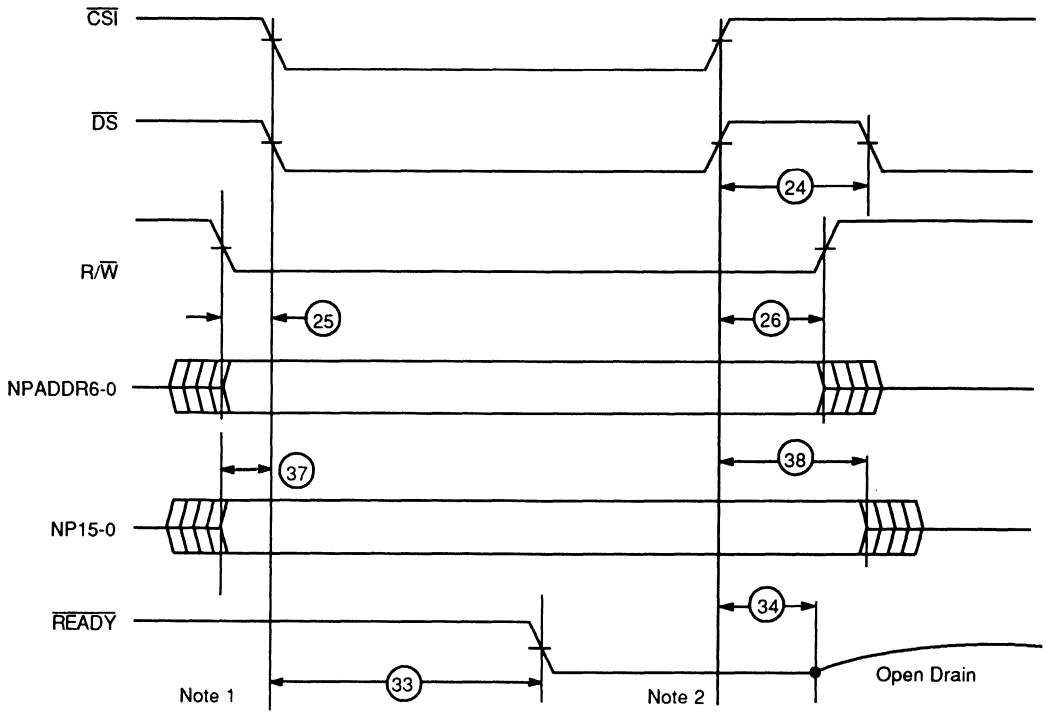
14977-041B

Notes:

1. 25, 28, 29, 33 are measured from $\overline{CSI}$ or $\overline{DS}$ whichever goes LOW last.
2. 26, 30, 31, 34 are measured from $\overline{CSI}$ or $\overline{DS}$ whichever goes HIGH first.

Figure 38. NP Bus Asynchronous Read Timings

SWITCHING WAVEFORMS



Notes:

1. 25, 37, 33 are measured from $\overline{CSI}$ or $\overline{DS}$ whichever goes LOW last.
2. 26, 38, 34 are measured from $\overline{CSI}$ or $\overline{DS}$ whichever goes HIGH first.

Figure 39. NP Bus Asynchronous Write Timings

SWITCHING WAVEFORMS

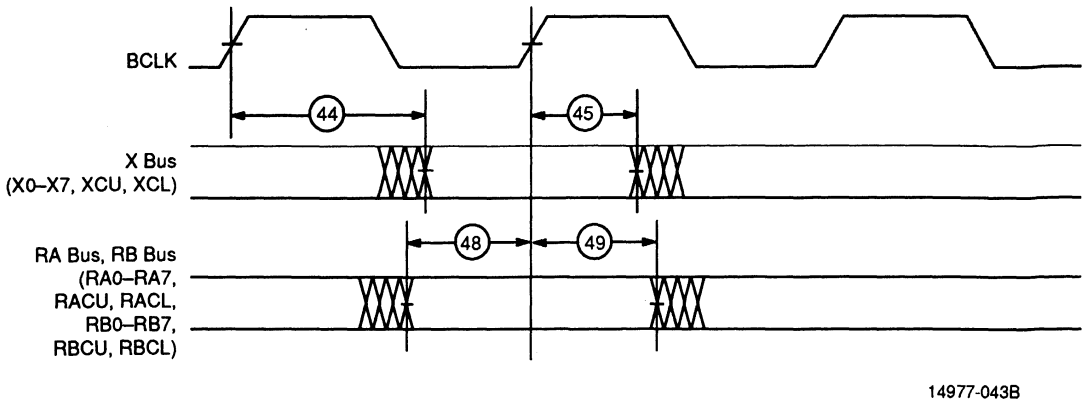


Figure 40. PHY Interface Timings

SWITCHING WAVEFORMS

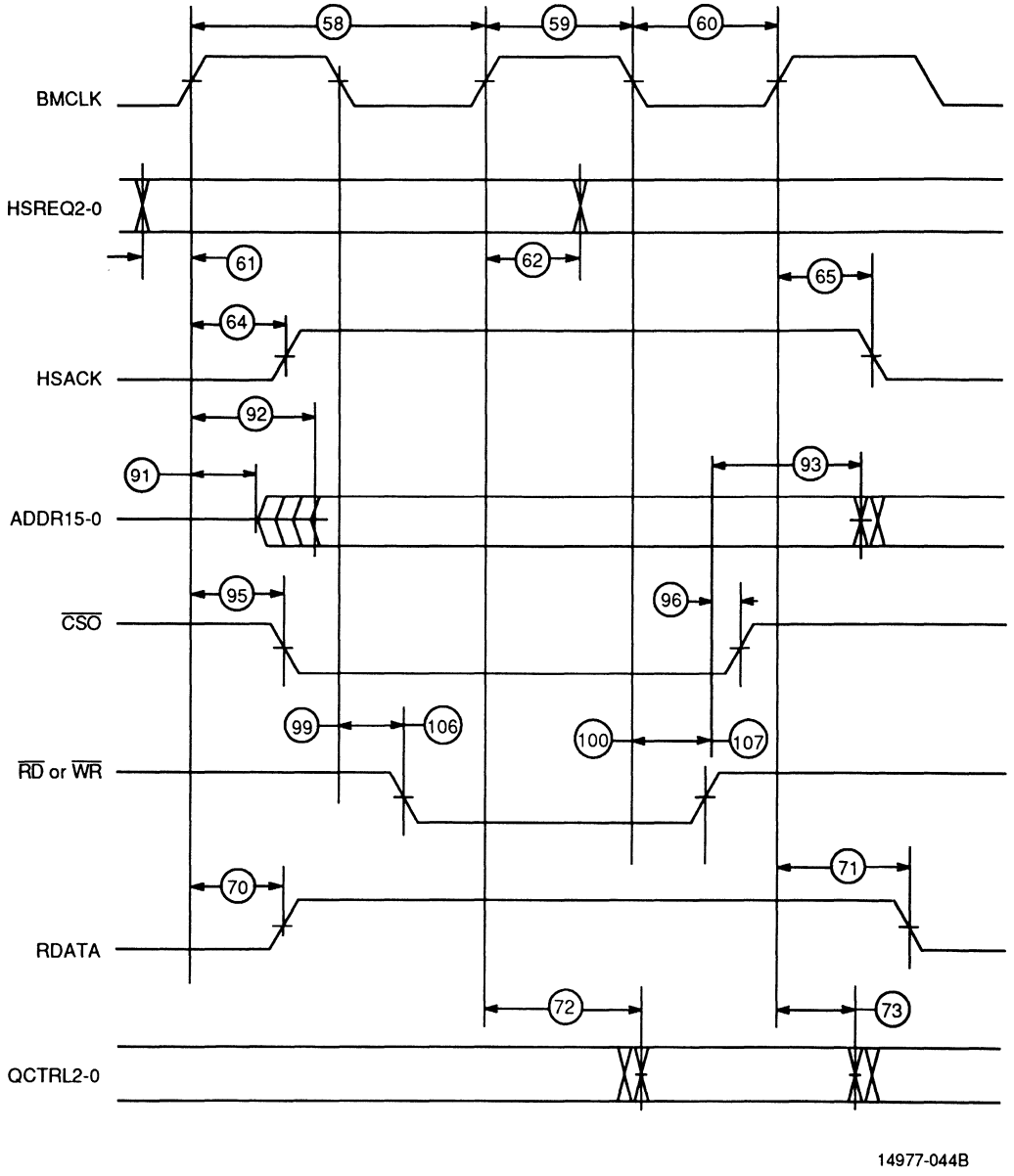


Figure 41. Host Interface Signal Timings

SWITCHING WAVEFORMS

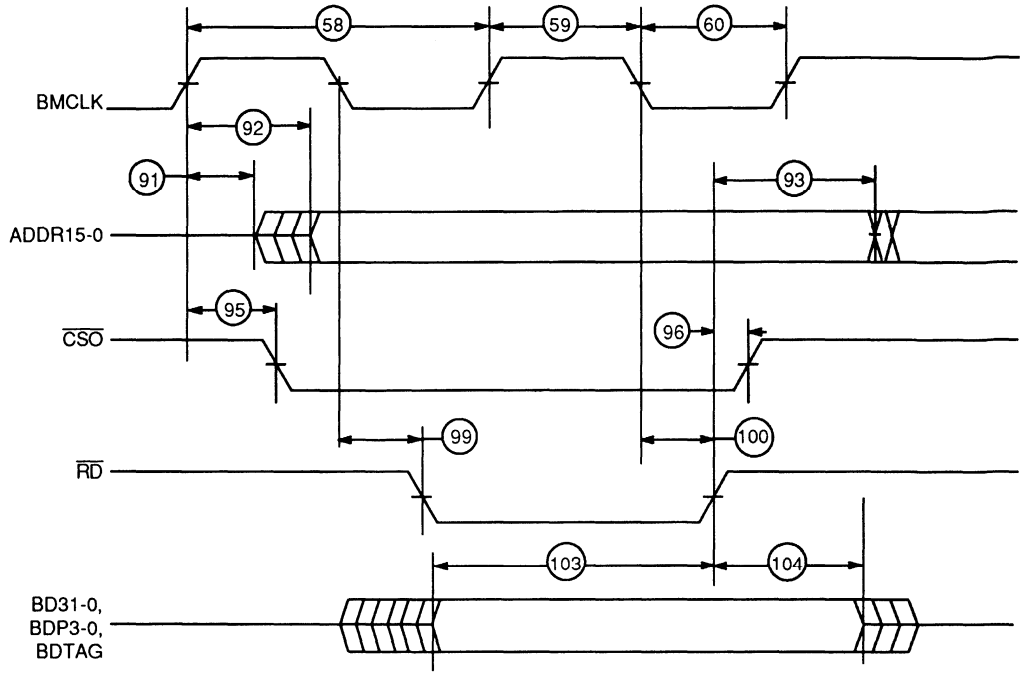


Figure 42. Buffer Memory Read Cycle Timings

SWITCHING WAVEFORMS

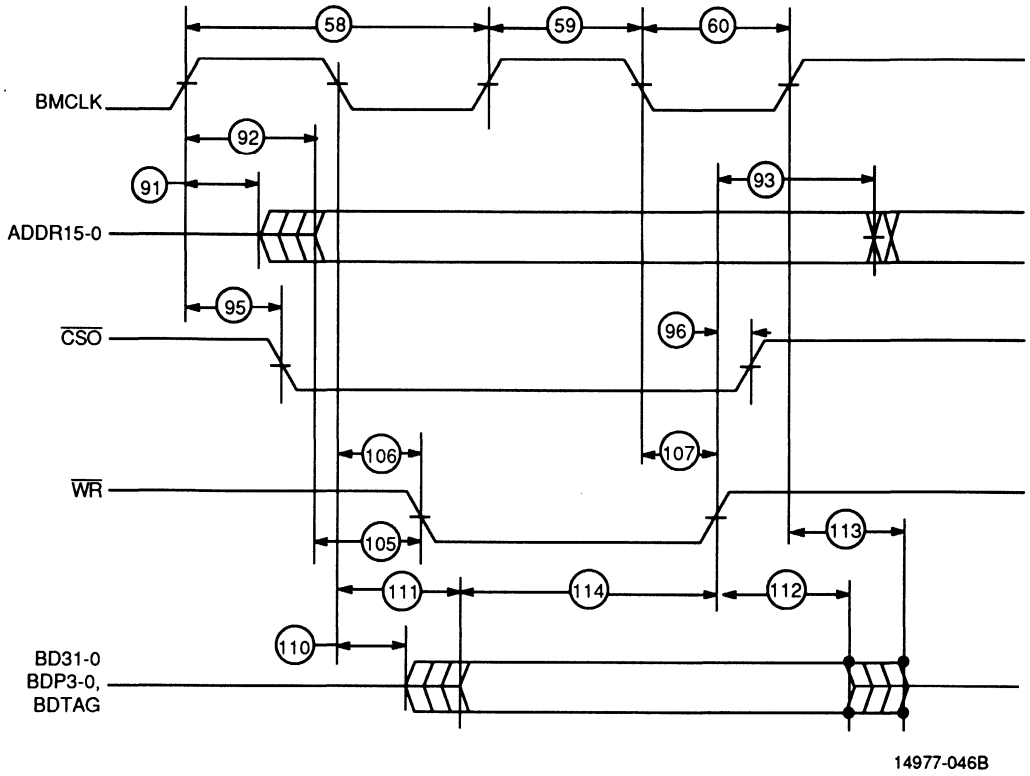


Figure 43. Buffer Memory Write Cycle Timings

SWITCHING WAVEFORMS

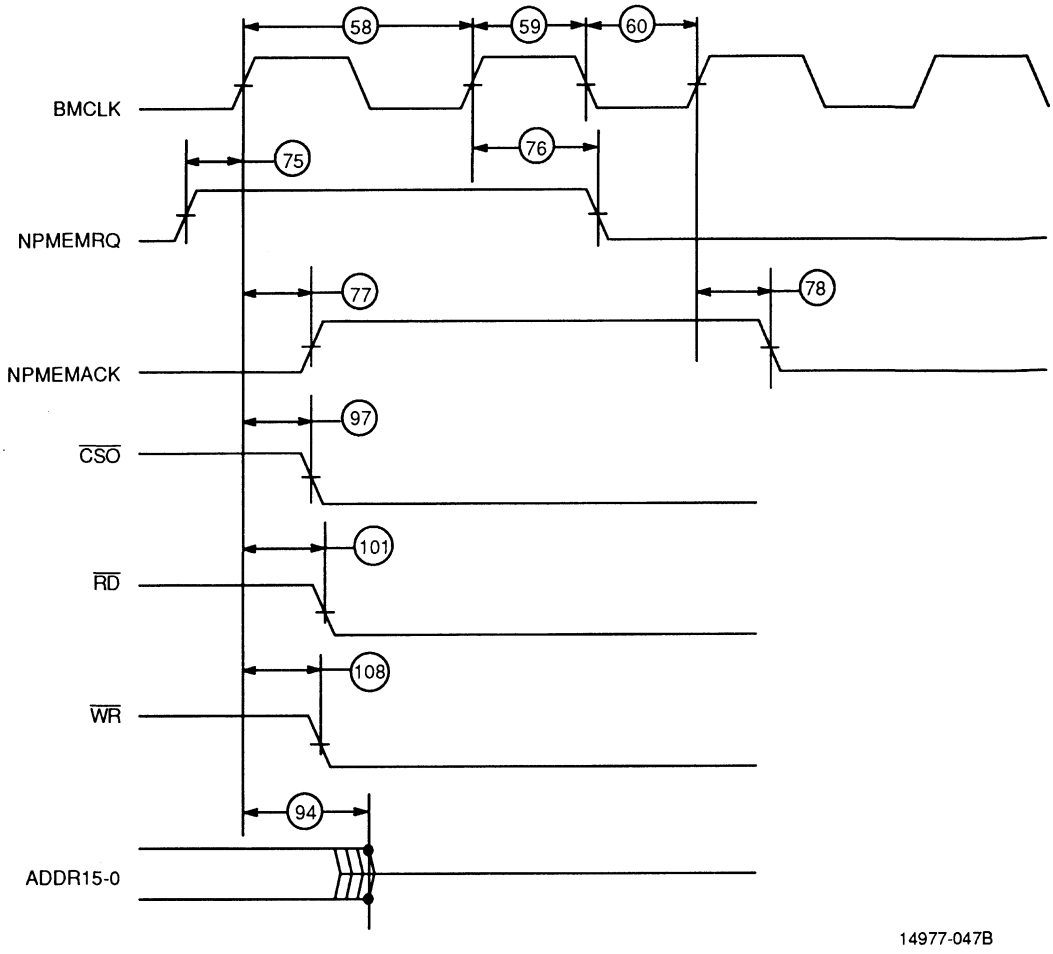


Figure 44. NP DMA Cycle Timings

SWITCHING WAVEFORMS

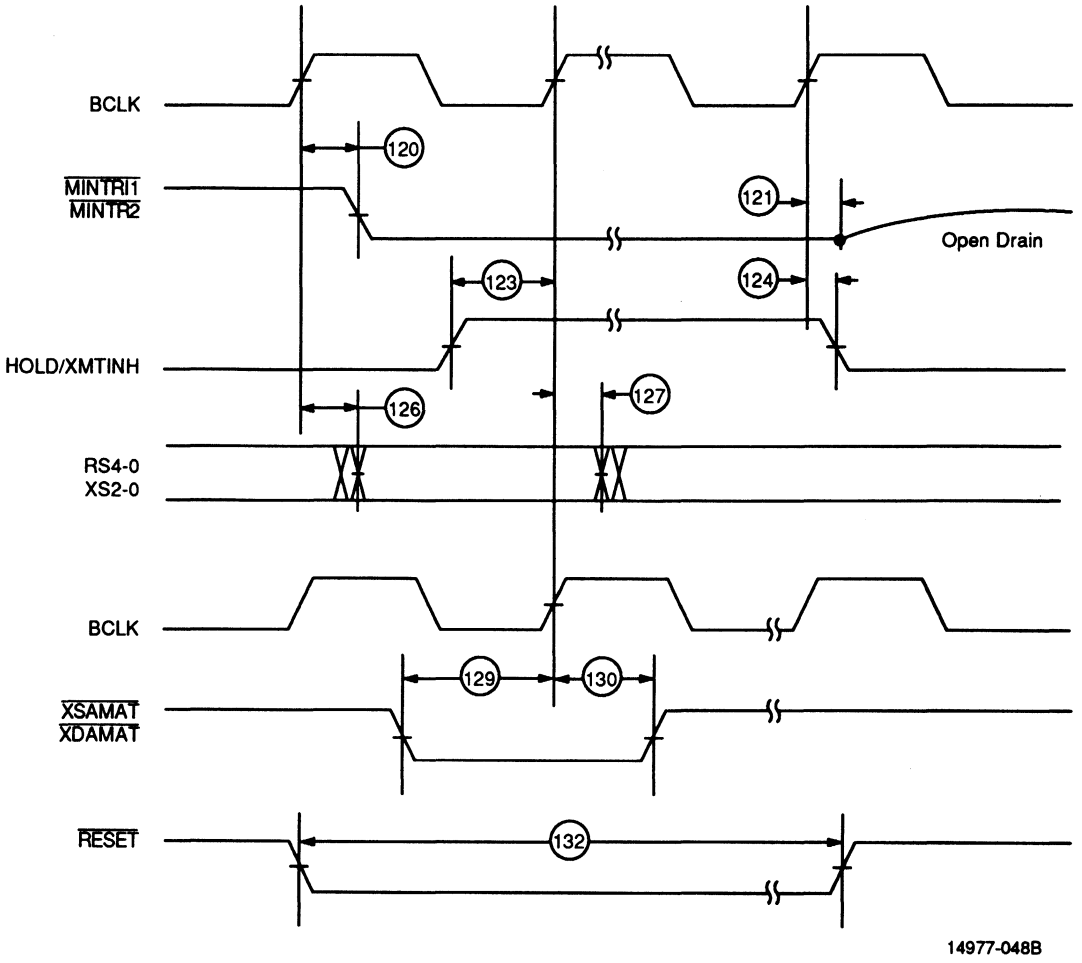
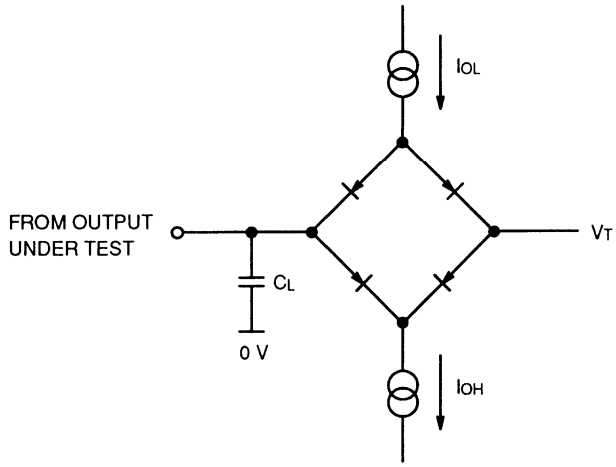


Figure 45. Timings of Miscellaneous Signals

SWITCHING TEST CIRCUIT



Notes:

C_L = 100 pF for the following pins:

BD31-0
BDTAG
BDP3-0
ADDR15-0
$\overline{CS0}$
$\overline{RD}$
$\overline{WR}$
$\overline{READY}$
$\overline{MINTR1}$
$\overline{MINTR2}$

14977-049A

C_L = 50 pF for all other bidirectional or output pins.

Standard Test Load

SWITCHING TEST WAVEFORMS

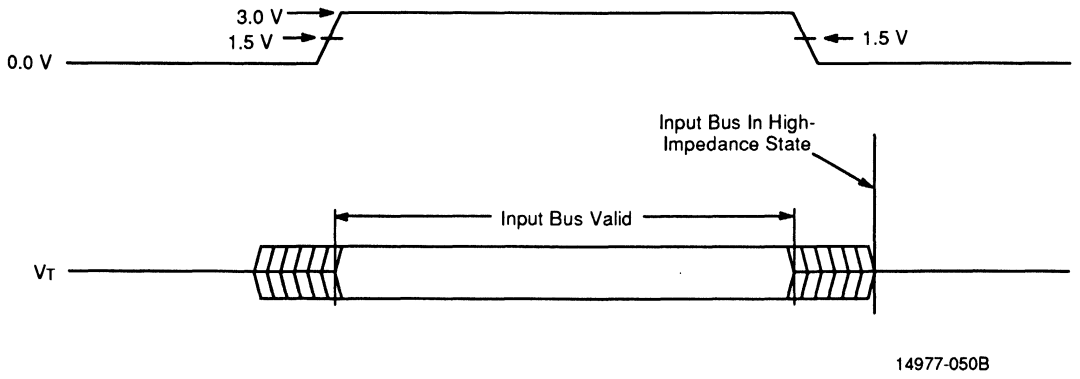


Figure 46. Input Waveform Test Points

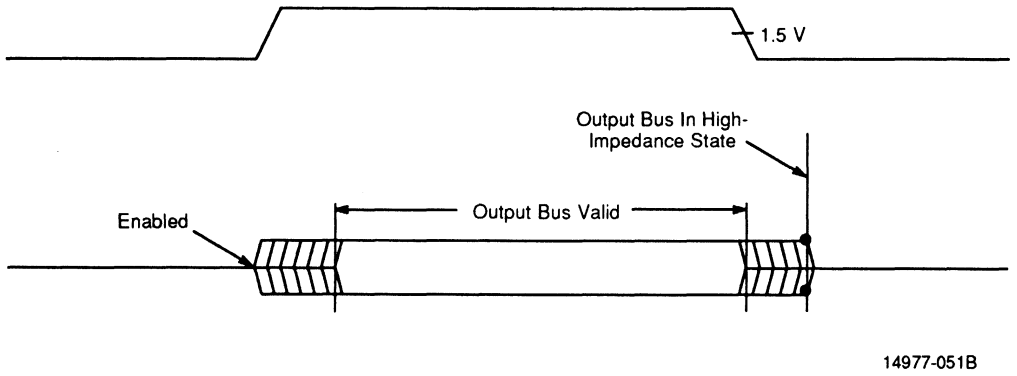


Figure 47. Output Waveform Test Points

APPENDIX A
GLOSSARY OF FORMAC Plus MNEMONICS

Introduction

The following table provides the meanings, equivalents, or definitions for each of the FORMAC Plus mnemonics used in this data sheet.

Mnemonic	Meaning
A	Address-match indicator field. Part of the E/A/C frame-status (FS) indicators at the end of each frame.
A0, A1, A2	Designations for the three asynchronous transmit queues.
ADDET2-0	Address detect. Bits10, 9, and 8 in MDREG1.
ADDR	Buffer memory address.
AFULL3-0	Almost-full; i.e. a preset binary value for the number of free long words left in the current transmit queue. Bits 3–0 in MDREG2.
$\overline{AS}$	Address strobe from NP (input). Active low.
ASYNC0	Asynchronous transmit queue 0.
ASYNC1	Asynchronous transmit queue 1.
ASYNC2	Asynchronous transmit queue 2.
BCLK	Byte clock. Runs the FORMAC Plus media-access logic. From 12.5 MHz external clock.
BD	Buffer-memory data bus (32 bits).
BDP3-0	Four-bit buffer-memory data-parity bus.
BDTAG	Buffer-memory tag-bit signal. Tag mode only.
BMCLCK	Buffer-memory clock input. for buffer memory use. From 12.5 MHz to 25 MHz external clock.
BMMODE	Buffer-memory-mode. Bit 15 in MDREG2. Tag or nontag mode.
C	Frame-copied indicator field. Part of the E/A/C frame-status (FS) indicators at end of frame.
CHKPAR	Check-parity-bit. Bit 13 in MDREG2.
CMDREG1	Command register 1.
CMDREG2	Command register 2.
CMT	Connection management.
CRC	Cyclic redundancy check. The 32-bit CRC value in the FCS field of a frame
$\overline{CSI}$	Chip-select input from NP. Active low.
$\overline{CSO}$	Chip-select-output command from address arbiter to buffer memory. Active low.
DA	Destination-address field in a frame.
DAS	Dual-attachment station on an FDDI ring.
DISCRY	Disable-carry bit. Bit 6 in MDREG1.
DISRCV	Disable receive state. Asserted when the ADDET2-0 bits in MDREG1 are in the 1 0 0 (binary) state.
DPC	Data path controller chip (Am79C82A)

GLOSSARY OF FORMAC Plus MNEMONICS (Continued)

Mnemonic	Meaning
$\overline{DS}$	Data strobe from NP (input). Active low.
E	Frame-error indicator field. Part of the E/A/C frame-status (FS) indicators at end of frame.
EAA0	End address of asynchronous transmit queue 0.
EAA1	End address of asynchronous transmit queue 1.
EAA2	End address of asynchronous transmit queue 2.
E/A/C	E, A, and C frame-status (FS) indicators (set to S or R) in the last three symbol fields of a frame.
EACB	End address of claim/beacon queue.
EARV	End address of receive queue.
EAS	End address of synchronous transmit queue.
ECNTR	16-bit error counter. Counts error frames.
ED	End delimiter field in frame (T symbol).
ENHSRQ	Enable-host-requests bit. (Bit 8 of MDREG2).
ENNPRQ	Enable-NP-DMA-requests bit. (Bit 7 of MDREG2).
ENRSF	Enable single-frame receive.
ERFBB1-0	Two bits indicating end of received-frame byte boundary. In receive-frame status word.
EXGPA1-0	Extended-group-addressing bits. (In MDREG1).
FC	Frame-control field in frame (indicates frame type).
FCNTR	16-bit frame counter. Counts received frames.
FCS	Frame-check sequence field in frame. Contains result of 32-bit CRC check of complete frame.
FDDI	Fiber Distributed Data Interface.
FIFO	Dual-port First-In/First-Out buffer for temporary data storage.
FORMAC	Fiber Optic Ring Media Access Controller (Am79C83).
FORMAC Plus	Single-chip Fiber Optic Ring Media Access Controller (Am79C830). Replaces and is downward compatible with the three-chip set: Am79C81A (RBC), Am79C82A (DPC), and Am79C83 (FORMAC).
FRMTHR	16-bit frame-threshold register.
FS	Frame-status field at end of frame. Contains E, A, and C indicators.
FULL/HALF	Full/half-duplex bit. (Bit 2 of MDREG1).
HOLD /XMTINH	Hold/transmit-inhibit.
HSACK	Host acknowledge: output to host.
HSREQ2-0	Host-request bus input. Specifies the type of buffer-memory access the host requires.

GLOSSARY OF FORMAC Plus MNEMONICS (Continued)

Mnemonic	Meaning
I	Frame preamble. Also known as an "idle" symbol. These symbols are transmitted between frames.
IFG	Interframe gap.
IMSK1	Interrupt-mask register for status register 1. IMSK1U is for upper 16 bits of ST1; IMSK1L is for lower 16 bits of ST1.
IMSK2	Interrupt-mask register for status register 2. IMSK2U is for upper 16 bits of ST2; IMSK2L is for lower 16 bits of ST2.
INFO	Designation for the information field in a frame.
IRMEMWI	Instruction: read memory with address increment.
IRMEMWO	Instruction: read memory without address increment.
LAGC	Long address, group (middle words of LAGP).
LAGL	Long address, group (LSW of LAGP).
LAGM	Long address, group (MSW of LAGP).
LAGP	Long address, group (complete 48-bit address).
LAIC	Long address, individual, (middle words of LAID).
LAID	Long address, individual (complete 48-bit address).
LAIL	Long address, individual (LSW of LAID).
LAIM	Long address, individual (MSW of LAID).
LCNTR	16-bit lost counter. Counts lost frames.
LLC	Link layer control.
LNCNL	Length count (in bytes) of next frame. This is the lower 8 bits of 16-bit length count. Nontag mode.
LNCNU	Length count (in bytes) of next frame. This is the upper 8 bits of 16-bit length count. Nontag mode.
LOCKTX	Lock-transmit-asynchronous-queues bit. In MDREG1.
LSB	Least-significant-byte bit. Bit 11 in MDREG2. The state of this bit determines the ordering of bytes in buffer-memory data frames.
LSW	Least significant word.
MA	My address; i.e. the address of this station.
MAC	This is the FDDI-defined Media Access Control (MAC) sublayer, defining frame structure, addressing, etc.
MARR	16-bit memory-address register for MDR random reads from buffer memory to NP.
MARW	16-bit memory-address register for MDR random writes from NP into buffer memory.
MDR	32-bit memory data register for random access of buffer memory by node processor.
MDREG1	16-bit mode-register 1.
MDREG2	16-bit mode-register 2.
MDRL	Lower 16 bits of 32-bit memory data register (MDR) for random access by NP.

GLOSSARY OF FORMAC Plus MNEMONICS (Continued)

Mnemonic	Meaning
MDRTAG	MDR tag bit. Bit 2 in MAC state-machine register.
MDRU	Upper 16 bits of 32-bit memory data register (MDR) for random access by NP.
$\overline{\text{MINTR1}}$	Maskable interrupt 1 to NP: Active low.
$\overline{\text{MINTR2}}$	Maskable interrupt 2 to NP: Active low.
MIR, MIR1 and MIR0	32-bit MAC information register. It is made up of the two 16-bit read-only registers: MIR1 and MIR0.
MMODE2-0	Three MDREG1 bits that control FORMAC Plus operational modes. (Bits 14–12 in MDREG1).
MORE	More frames in queue. Nontag mode.
MSRABT	Memory-status-receive-abort bit. Bit 30 in receive-frame status word.
MSVALID	Memory-status-valid bit. In receive-frame status word.
MSW	Most significant word.
NFCS	No FCS; i.e., do not append four-byte frame-check sequence (FCS) at end of transmit frame.
NP	Designation for the node processor; or a designation for the 16-bit data bus from the node processor (input).
NPADDR	Input from the 7-bit NP address bus.
NPMEMACK	NP memory access acknowledge output (to NP DMA logic).
NPMEMRQ	NP memory request input (from NP DMA logic).
NPMODE	NP bus mode (input).
NSA	Next station address (used in SMT).
OSI	Open Systems Interconnection communication model.
PARITY	Parity-type bit (1 = even parity). Bit 12 in MDREG2.
PHY	Physical protocol sublayer (per FDDI): encodes and decodes data moving between the FORMAC Plus and the physical media.
PMD	Physical-media-dependent sublayer (per FDDI): i.e. the optical interconnecting components that convert light signals to/from electrical signals.
PRI0, PRI1 and PRI2	Designations for three 16-bit registers containing the assigned transmit-priority values for the three corresponding asynchronous transmit queues.
QCTRL2-0	Buffer-memory three-bit queue-control output to host. Tag mode only.
R	Reset state of the E, A, or C indicator in the frame status (FS) field of a frame.
RA	Receive bus A (input from PHY). Each nibble contains either data or a network control character.
RACL	Receive A control line for lower nibble of RA bus (input from PHY). High = network control character. Low = data
RACU	Receive A control line for upper nibble of RA bus (input from PHY). High = network control character. Low = data
RB	Receive bus B (input from PHY). Each nibble contains either data or a network control character.

GLOSSARY OF FORMAC Plus MNEMONICS (Continued)

Mnemonic	Meaning
RBC	RAM buffer controller chip (Am79C81A).
RBCL	Receive B control line for lower nibble of RB bus (input from PHY). High = network control character. Low = data
RBCU	Receive B control line for upper nibble of RB bus (input from PHY). High = network control character. Low = data
RCVERR	Receive-errored-frames bit. Bit 4 of MDREG2.
RDATA	Receive data output signal to host. Tag mode only.
$\overline{RD}$	Buffer memory read command. Active low.
$\overline{READY}$	Ready output to NP (read/write acknowledgment that data transfer is complete). Active low.
RPR	Read-pointer for receive queue.
RPXA0	Read-pointer for transmit asynchronous queue 0.
RPXA1	Read-pointer for transmit asynchronous queue 1.
RPXA2	Read-pointer for transmit asynchronous queue 2.
RPXL	Read-pointer transmit lower. This is the lower 8 bits of the 16-bit address of the descriptor for the next transmit frame. Nontag mode only.
RPXS	Read-pointer for transmit synchronous queue.
RPXSF	Read-pointer for transmitting special frames.
RPXU	Read-pointer transmit upper. This is the upper 8 bits of the 16-bit address of the descriptor for the next transmit frame. Nontag mode only.
RS	Receive-status output.
$\overline{RST}$	Reset-input from external source. Active low. Initializes FORMAC Plus state machines and registers.
RTHR	4-bit receive-frame threshold value in the 16-bit FRMTHR register. Tag mode.
R/$\overline{W}$	Input line selecting read or write access between FORMAC Plus and NP.
RXFBB1-0	Receive-frame byte boundary. Bits 9 and 10 in MDREG2.
S	Reset state of the E, A, or C indicator in the frame status (FS) field of a frame.
SA	Source-address field in frame.
SABC	Start-address of beacon frame.
SACL	Start-address of claim frame.
SADET	Status: address detect.
SADRRG	Status: internal-address-recognized bit. In receive-frame status word.
SAGP	Short address, group (16-bit address).
SAID	Short address, individual (16-bit address).
SAS	Single attachment station on an FDDI ring.
SCLM	Status: claim-state entered. Bit 6 of ST2U.
SD	Start-delimiter field in a frame (contains J and K symbols).
SDUPCLM	Status: duplicate claim. Bit 2 of ST2L.

GLOSSARY OF FORMAC Plus MNEMONICS (Continued)

Mnemonic	Meaning
SEAC2-0	Three bits indicating the set/reset status of the received E, A and C frame-status indicators.
SELRA	If SELRA bit = logic 1 (high), then RA bus input from PHY is selected. If SELRA = logic 0 (low), then RB bus is selected as input from PHY. (In MDREG1).
SELSA	Select-short-address bit. Bit 11 of MDREG1.
SERRSF	Status: error in special frame. Bit 7 of ST2U.
SERRCTR	Status: error counter overflow. Bit 5 of ST2L.Set when the 16-bit error counter (ECNTR) overflows.
SFRMCTR	Status: frame counter overflow. Bit 4 of ST2L.Set when the 16-bit frame counter (FCNTR) overflows.
SFRMTY2-0	Status: frame-type. In receive-frame status word.
SHICLM	Status: high claim. Bit 4 of ST2U.
SLOCLM	Status: lower claim. Bit 3 of ST2U.
SLSTCTR	Status: lost counter. Bit 6 of ST2L.Set when the 16-bit lost counter (LCNTR) overflows.
SMISFRM	Status: missed frame. Bit 9 of ST2L.
SMT	Station management. A portion of FDDI affecting the individual sublayers and involving ring configuration, error detection, and fault isolation.
SMULTDA	Status: multiple destination address. Bit 14 of ST2L.
SMYBEC	Status: my beacon. Bit 1 of ST2U.
SMYCLM	Status: my claim. Bit 5 of ST2U.
SNFSLD	Status: NP/FORMAC Plus simultaneous load. In ST2U.
SNGLFRM	Single-frame-receive-mode. Bit 15 in MDREG1.
SNPPND	Status: node-processor MDR read or write request pending. This is bit 3 of MAC state-machine register.
SOTRBEC	Status: other beacon. Bit 0 of ST2U.
SPCEPD (S, A0, A1, A2)	Status: parity/coding error in pointer, or descriptor, or data (synchronous queue, asynchronous queue 0, async1 and async2).
SPHINV	Status: PHY invalid. Bit 7 of ST2L.
SQLCK (S, A0, A1, A2)	Status: queue-lock (synchronous queue, asynchronous queue 0, asynchronous queue1, and asynchronous queue 2). Bits 0–3 of ST1L.
SRABT	Status: receive abort. Bit 13 of ST2U.
SRBFL	Status: receive buffer full. Bit 12 of ST2U.
SRBMT	Status: receive buffer empty. Bit 14 of ST2U.
SRCOMP	Status: receive complete. Nontag mode. Bit 15 of ST2U.
SRCVFRM	Status: receive single frame. Bit 10 of ST2U.
SRCVOVR	Status: receive FIFO overflow. Bit 11 of ST2U.
SRFRCTOV	Status: receive frame counter overflow. Bit 9 of ST2U.
SRNGOP	Status: ring operational. Bit 15 of ST2L.

GLOSSARY OF FORMAC Plus MNEMONICS (Continued)

Mnemonic	Meaning
SSIFG	Status: short interframe gap. Bit 3 of ST2L.
SSRCRTG	Status: source-routing bit. Set if source address (SA) of frame has MSB set. Bit 28 in receive-frame status word.
ST1, ST1U and ST1L	32-bit Status Register 1. Divided into two separately addressable 16-bit upper and lower halves designated ST1U and ST1L.
ST2, ST2U and ST2L	32-bit Status Register 2. Divided into two separately addressable 16-bit upper and lower halves designated ST2U and ST2L.
STBFLA	Status: transmit buffer full, asynchronous queues. Tag mode only. Bit 9 of ST1U.
STBFLS	Status: transmit buffer full, synchronous queue. Tag mode only. Bit 10 of ST1U.
STBUR (S, A0, A1, A2)	Status: transmit buffer underrun (synchronous, async0, async1, and async2 queues). Bits 12–15 of ST1L.
STECFRM (S, A0, A1, A2)	Status: transmit end of chain of frames (synchronous, async0, async1, and async2 queues). Bits 4–7 of ST1U.
STEFRM (S, A0, A1, A2)	Status: transmit end of frame (synchronous, async0, async1, and async2 queues). Bits 0–3 of ST1U.
STEXDONS	Status: transmit until "XDONE" in synchronous queue.
STKERR	Status: token error. Bit 13 of ST2L.
STKISS	Status: token issued. Bit 12 of ST2L.
STMCHN	State machine register.
STRPFCS	Strip frame-check-sequence (CRC) bit. In MDREG2.
STRTEXP	Status bit set when TRT (token rotation timer) expires and late count is greater than 0. Bit 10 of ST2L.
STRTEXR	Status bit set when TRT expires in recovery, i.e. when transmit state-machine is in T4 or T5 state. Bit 1 of ST2L.
STVXEXP	Status: TVX (valid transmission timer) expired. Bit 11 of ST2L.
STXABR (S, A0, A1, A2)	Status: transmit abort due to reset or recovery. (synchronous, async0, async1, async2 queues).
STXINFL (S, A0, A1, A2)	Status: transmit instruction full (synchronous, async0, async1, and async2 queues).
SWPR	Shadow write pointer for receive queue.
SWPXA0	Shadow write pointer: transmit asynchronous queue 0.
SWPXA1	Shadow write pointer: transmit asynchronous queue 1.
SWPXA2	Shadow write pointer: transmit asynchronous queue 2.
SWPXS	Shadow write pointer: transmit synchronous queue.
SXMTABT	Status: transmit abort. Bit 15 of ST1U.
SYMCTL	Symbol-control bit. Bit 5 of MDREG2.
SYNPRQ	Synchronous-NP-DMA-request-bit. Bit 6 of MDREG2.
T	End-delimiter symbol in a frame.

GLOSSARY OF FORMAC Plus MNEMONICS (Continued)

Mnemonic	Meaning
THT	21-bit token-hold timer.
TM0, TM1	Token-mode bits. These are bits 10 and 11 of the 16-bit MAC state-machine register (read only).
TMAX	Default token-rotation time loaded into TRT after recovery, reset or initialization.
TMRS	16-bit read-only timer register holding token-timing information.
TMSYNC	21-bit timer loaded with TSYNC value at the start of synchronous transmission.
TNEG	Negotiated token-rotation time (TRT).
TOPR	Operational time. This is the initial value (i.e. current in-use value) of TRT as set by the claim process.
TPRI	Stores and checks priority for the three asynchronous queues.
TREQ	Requested TRT (contained in two 16-bit registers: TREQ0 and TREQ1)
TRT	21-bit token-rotation timer.
TSYNC	Synchronous transmission bandwidth.
TTRT	Target TRT for the ring.
TVX	8-bit timer counting expected time between valid transmissions.
TXFBB1-0	Transmit-frame byte boundary. Bits 28 and 27 in buffer-memory transmit descriptor.
WPR	Write-pointer for receive queue.
WPSF	Write-pointer special frames.
WPXA0	Write-pointer for transmit asynchronous queue 0.
WPXA1	Write-pointer for transmit asynchronous queue 1.
WPXA2	Write-pointer for transmit asynchronous queue 2.
WPXS	Write-pointer for transmit synchronous queue.
WPXSF	Write-pointer for transmit special frames.
$\overline{WR}$	Buffer-memory write signal (output). Active low.
X	FORMAC Plus 8-bit transmit bus (output to PHY).
XCL	Transmit control, lower nibble of X bus (output to PHY). High = network control character. Low = data.
XCU	Transmit control, upper nibble of X bus (output to PHY). High = network control character. Low = data.
$\overline{XDAMAT}$	External-destination address-match input. Active low. (From external address-match logic).
XDONE	Transmit done.
XMTABT	Transmit abort.
XMTINH /HOLD	Hold/transmit-inhibit bit. Bit 1 of MDREG1. This is also the name of the hold/transmit-inhibit input signal from external special-purpose logic.
XS	Transmit-status output.
$\overline{XSAMAT}$	External-source address-match input. Active low. (From external address match logic).
XTHR	12-bit transmit-frame threshold value in the 16-bit FRMTHR register. Tag mode only.

APPENDIX B

SUMMARY TABLES DESCRIBING FORMAC Plus Status Registers and Mode Registers

Status Register 1, Upper 16 Bits (ST1U)

Bit Mnemonic	Bit Position	Description or Function
SXMTABT	15	Status: transmit-abort.
STXABRA2	14	Status: asynchronous queue 2 transmit-abort due to reset or recovery.
STXABRA1	13	Status: asynchronous queue 1 transmit-abort due to reset or recovery.
STXABRA0	12	Status: asynchronous queue 0 transmit-abort due to reset or recovery.
STXABRS	11	Status: synchronous queue transmit-abort due to reset or recovery.
STBFLS	10	Status: synchronous-queue transmit-buffer full.
STBFLA	9	Status: asynchronous-queue transmit-buffer full.
STEXDONS	8	Status: transmit until XDONE in synchronous queue.
STECFRMA2	7	Status: transmit end of chain of asynchronous-queue–2 frames.
STECFRMA1	6	Status: transmit end of chain of asynchronous-queue–1 frames.
STECFRMA2	5	Status: transmit end of chain of asynchronous-queue–0 frames.
STECFRMS	4	Status: transmit end of chain of synchronous-queue frames.
STEFRMA2	3	Status: transmit end of frame: asynchronous queue 2.
STEFRMA1	2	Status: transmit end of frame: asynchronous queue 1.
STEFRMA0	1	Status: transmit end of frame: asynchronous queue 0.
STEFRMS	0	Status: transmit end of frame: synchronous queue.

Status Register 1, Lower 16 Bits (ST1L)

Bit Mnemonic	Bit Position	Description or Function
STBURA2	15	Status: transmit-buffer underrun: asynchronous queue 2.
STBURA1	14	Status: transmit-buffer underrun: asynchronous queue 1.
STBURA0	13	Status: transmit-buffer underrun: asynchronous queue 0.
STBURS	12	Status: transmit-buffer underrun: synchronous queue.
SPCEPDA2	11	Status: parity/coding error in pointer, or descriptor, or data: asynchronous queue 2.
SPCEPDA1	10	Status: parity/coding error in pointer, or descriptor, or data: asynchronous queue 1.
SPCEPDA0	9	Status: parity/coding error in pointer, or descriptor, or data: asynchronous queue 0.
SPCEPDS	8	Status: parity/coding error in pointer, or descriptor, or data: synchronous queue.
STXINFLA2	7	Status: transmit instruction full: asynchronous queue 2.
STXINFLA1	6	Status: transmit instruction full: asynchronous queue 1.
STXINFLA0	5	Status: transmit instruction full: asynchronous queue 0.
STXINFLS	4	Status: transmit instruction full: synchronous queue.
SQLCKA2	3	Status: queue lock for asynchronous queue 2.
SQLCKA1	2	Status: queue lock for asynchronous queue 1.
SQLCKA0	1	Status: queue lock for asynchronous queue 0.
SQLCKS	0	Status: queue lock for synchronous queue.

Status Register 2, Upper 16 Bits (ST2U)

Bit Mnemonic	Bit Position	Description or Function
SRCOMP	15	Status: receive complete. Nontag mode.
SRBMT	14	Status: receive buffer empty.
SRABT	13	Status: receive abort.
SRBFL	12	Status: receive buffer full.
SRCVOVR	11	Status: receive FIFO overflow.
SRCVFRM	10	Status: receive frame.
SRFRCTOV	9	Status: receive frame counter overflow.
SNFSLD	8	Status: Node processor and FORMAC Plus simultaneous load.
SERRSF	7	Status: error in special frame.
SCLM	6	Status: claim state entered.
SMYCLM	5	Status: my claim received.
SHICLM	4	Status: high claim received.
SLOCLM	3	Status: low claim received.
SBEC	2	Status: beacon state entered.
SMYBEC	1	Status: my beacon received.
SOTRBEC	0	Status: other beacon received.

Status Register 2, Lower 16 Bits (ST2L)

Bit Mnemonic	Bit Position	Description or Function
SRNGOP	15	Status: ring operational.
SMULTDA	14	Status: multiple destination address.
STKERR	13	Status: token error.
STKISS	12	Status: token issued.
STVXEXP	11	Status: TVX expired.
STRTEXP	10	Status: TRT expired and late count greater than 0.
SMISFRM	9	Status: missed frame.
SADET	8	Status: address detect.
SPHINV	7	Status: PHY invalid.
SLSTCTR	6	Status: lost counter overflow.
SERRCTR	5	Status: error counter overflow.
SFRMCTR	4	Status: frame counter overflow.
SSIFG	3	Status: short interframe gap.
SDUPCLM	2	Status: duplicate claim received.
STRTEXR	1	Status: TRT expired in claim or beacon state.
——	0	Reserved.

Mode Register 1 (MDREG1)

Bit Mnemonic	Bit Position	Description or Function
SNGLFRM	15	Single-frame-receive mode.
MMODE2	14	Control FORMAC Plus operational modes (bit 2).
MMODE1	13	Control FORMAC Plus operational modes (bit 1).
MMODE0	12	Control FORMAC Plus operational modes (bit 0).
SELSA	11	Select-short-address bit
ADDET2	10	Address-detect bit 2.
ADDET1	9	Address-detect bit 1.
ADDET0	8	Address-detect bit 0.
SELRA	7	Select input from PHY. 1 = input from RA. 0 = input from RB.
DISCRY	6	Disable-carry bit.
EXGPA1	5	Extended-group-addressing bit 1.
EXGPA0	4	Extended-group-addressing bit 0.
LOCKTX	3	Lock-transmit-asynchronous-queues bit.
FULL/HALF	2	Full-duplex/half-duplex bit.
XMTINH/HOLD	1	Transmit-inhibit/hold bit.
——	0	Reserved.

Mode Register 2 (MDREG2)

Bit Mnemonic	Bit Position	Description or Function
BMMODE	15	Buffer-memory-mode bit.
STRPFCS	14	Strip-frame-check-sequence (CRC) bit.
CHKPAR	13	Check-parity bit.
PARITY	12	Parity type: 1 = even; 0 = odd.
LSB	11	The state of the LSB bit determines the ordering of bytes in buffer-memory data frames.
RXFBB1	10	Receive frame byte boundary (bit 1).
RXFBB0	9	Receive frame byte boundary (bit 0).
ENHSRQ	8	Enable-host-request bit.
ENNPRQ	7	Enable-NP-DMA-request bit.
SYNPRQ	6	Synchronous-NP-DMA-request bit.
SYMCTL	5	Symbol-control bit.
RCVERR	4	Receive-errored-frames bit.
AFULL3	3	Transmit queue almost-full value, bit 3.
AFULL2	2	Transmit queue almost-full value, bit 2.
AFULL1	1	Transmit queue almost-full value, bit 1.
AFULL0	0	Transmit queue almost-full value, bit 0.

Preliminary

Am79C864

Physical Layer Controller (PLC)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Implements FDDI PHY layer protocol for ISO standard (FDDI) 9314-1
- Hardware Physical Connection Management (PCM) support
- Performs Physical Connection insertion and removal
- Onchip Link Error Monitor (LEM) and Link Confidence Test (LCT)
- Line state detection
- Repeat Filter
- Elasticity Buffer and Smoother functions
- 4B/5B Encoding/Decoding
- Full Duplex Operation
- Data Framing
- Built-in Self Test

GENERAL DESCRIPTION

The Physical Layer Controller (PLC) is a CMOS device which along with Physical Data Transmitter (PDT) and Physical Data Receiver (PDR) implements the Physical Layer Protocol (PHY) and portions of the Station Management (SMT) of the ANSI Fiber Distributed Data Interface (FDDI) standard. The PLC, PDT and PDR are collectively known as the AmPHY. PHY functions performed by the PLC include framing of data on symbol pair boundaries, the elasticity buffer function, the smoothing function, 4B/5B encoding and decoding of symbols, line state detection and the repeat filter function. SMT functions performed include Physical Connection Management (PCM), Physical Connection insertion and removal and Link Error Monitor.

The PLC chip receives symbol-wide (5 bits) data along with a 25 MHz recovered clock from the PDR chip and searches for a JK symbol pair (also known as Starting Delimiter). It uses the starting delimiter to establish byte boundaries (i.e. to frame the data).

Framed data is then sent to the Elasticity Buffer which serves to compensate for the frequency difference between the recovered clock and the local clock. Data output by the Elasticity Buffer is checked by the Smoother and when necessary, Idle symbols are inserted between frames to maintain a minimum number of Idle symbols in the interframe gap.

The data is then decoded and sent to the Media Access Control (MAC) chip. The data is byte-wide (10 bits) and is clocked by a 12.5 MHz local clock.

The PLC receives byte-wide data from the MAC at 12.5 million bytes per second, encodes the data and sends out symbol-wide data at 25 million symbols per second to PDT chip. In the transmit path, there is a Repeat Filter to detect corrupted symbols and convert them into the specified pattern of Halt and Idle symbols. The Repeat Filter in each PLC chip converts the last byte of a frame fragment into Idle symbols and thus eventually removing fragments from the ring.

The PCM initializes the connection of neighboring PHYs and manages the PHY signaling. PCM consists of the PCM state machine, which determines the timing and state requirements for PCM, and the PCM Pseudo Code, which provides the information to be communicated to the neighboring PCM and specifies the connection policies. The PLC chip contains the PCM State Machine, while the PCM Pseudo Code is controlled by software. The PCM State Machine communicates with other PCMs using a bit signaling mechanism whereby certain line states are received and transmitted. The PCM also makes use of the Link Error Monitor in the PLC chip during Link Confidence Test and after the link has been formed, to detect a noisy link. The PLC contains a Line State Machine for detecting received line states and a Data Stream Generator for transmitting the various line states. The PLC also contains a state machine called Physical Connection Insertion (PCI) which is used in Physical Connection insertion and removal. It performs the necessary ring scrubbing and data path switching.

The Node Processor Interface in the PLC consists of several control and status registers. The PLC also contains error and special event counters, Built In Self Test (BIST) logic, Boundary Scan logic, and several data loopback multiplexers so that internal data paths may be reconfigured for test purposes.

Publication# 15535 Rev. A Amendment/0
Issue Date: September 1991

BLOCK DIAGRAM

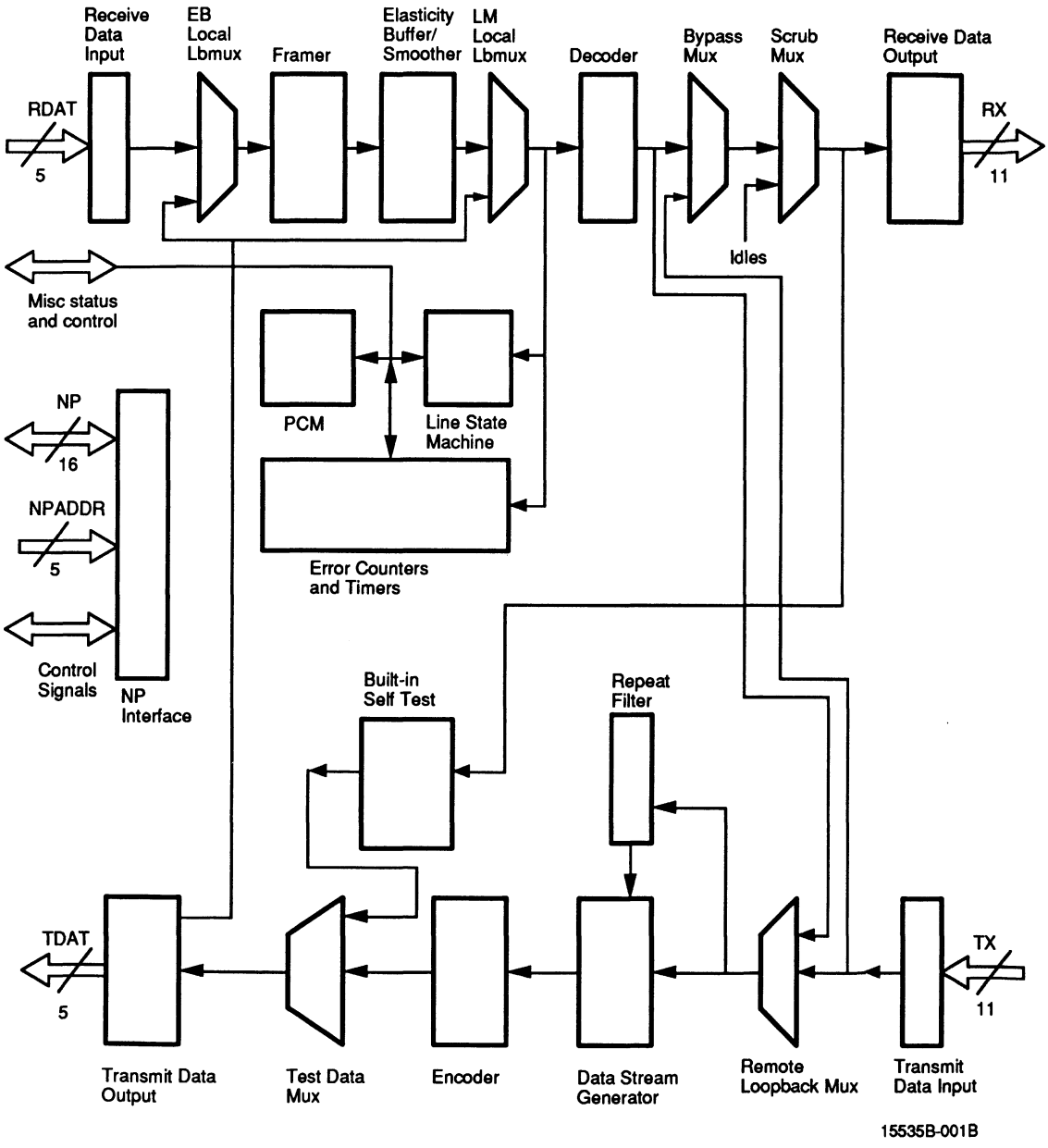


TABLE OF CONTENTS

DISTINCTIVE CHARACTERISTICS 3-1

GENERAL DESCRIPTION 3-1

BLOCK DIAGRAM 3-2

TABLE OF CONTENTS 3-3

CONNECTION DIAGRAM 3-5

PIN DESIGNATIONS 3-6

LOGIC SYMBOL 3-7

ORDERING INFORMATION 3-8

PIN DESCRIPTION 3-9

FUNCTIONAL DESCRIPTION 3-12

Node Processor Interface 3-12

Read Cycle 3-12

Write Cycle 3-12

Registers 3-15

PLC Control and Status Registers 3-15

Physical Connection Management Timers 3-23

Physical Connection Management Timing Parameters 3-24

Physical Connection Management Bit Signaling Registers 3-25

Event Counters 3-26

Interrupt Registers 3-27

Built In Self Test Register 3-29

Framer 3-29

Elasticity Buffer 3-29

Smoother Operation 3-29

Line State Machine (LSM) 3-30

Link Error Monitor 3-31

Physical Connection Management (PCM) 3-32

PCM Operation 3-33

PCM State Machine 3-33

Pseudo Code Bit Signaling 3-33

PCI Operation 3-36

PCI State Machine 3-37

TABLE OF CONTENTS

Decoder 3-38

Encoder 3-39

Repeat Filter 3-40

Data Stream Generator 3-40

Data Path MUXes 3-40
- EB Local Loopback MUX 3-41
- LM Local Loopback MUX 3-41
- Bypass MUX 3-41
- Remote Loopback MUX 3-41
- Scrub MUX 3-41
- Test Data MUX 3-41

Data Input/Output 3-41
- Receive Data Input 3-41
- Receive Data Output 3-42
- Transmit Data Input 3-42
- Transmit Data Output 3-42

Built In Self Test (BIST) 3-42
- BIST Operation 3-42
- Counter Segmentation Test Mode 3-43
- Boundary Scan Test Mode 3-43

ABSOLUTE MAXIMUM RATINGS 3-44

OPERATING RANGES 3-44

DC CHARACTERISTICS 3-44

CAPACITANCE 3-44

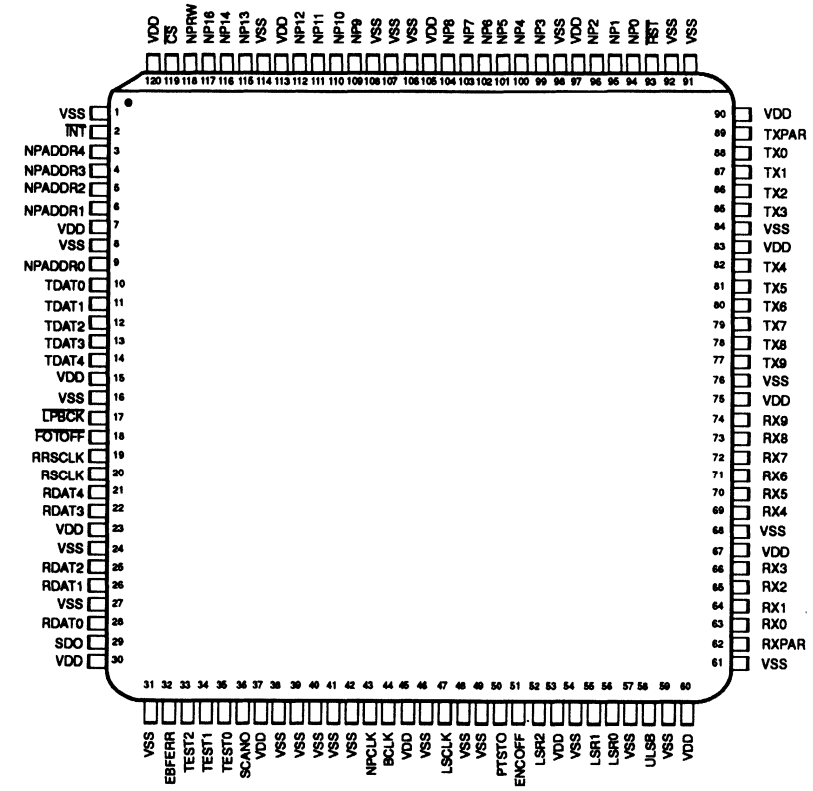
SWITCHING CHARACTERISTICS 3-45

SWITCHING WAVEFORMS 3-46

SWITCHING TEST CIRCUITS 3-50

SWITCHING TEST WAVEFORMS 3-51

CONNECTION DIAGRAM
120-Pin PQFP (Top View)

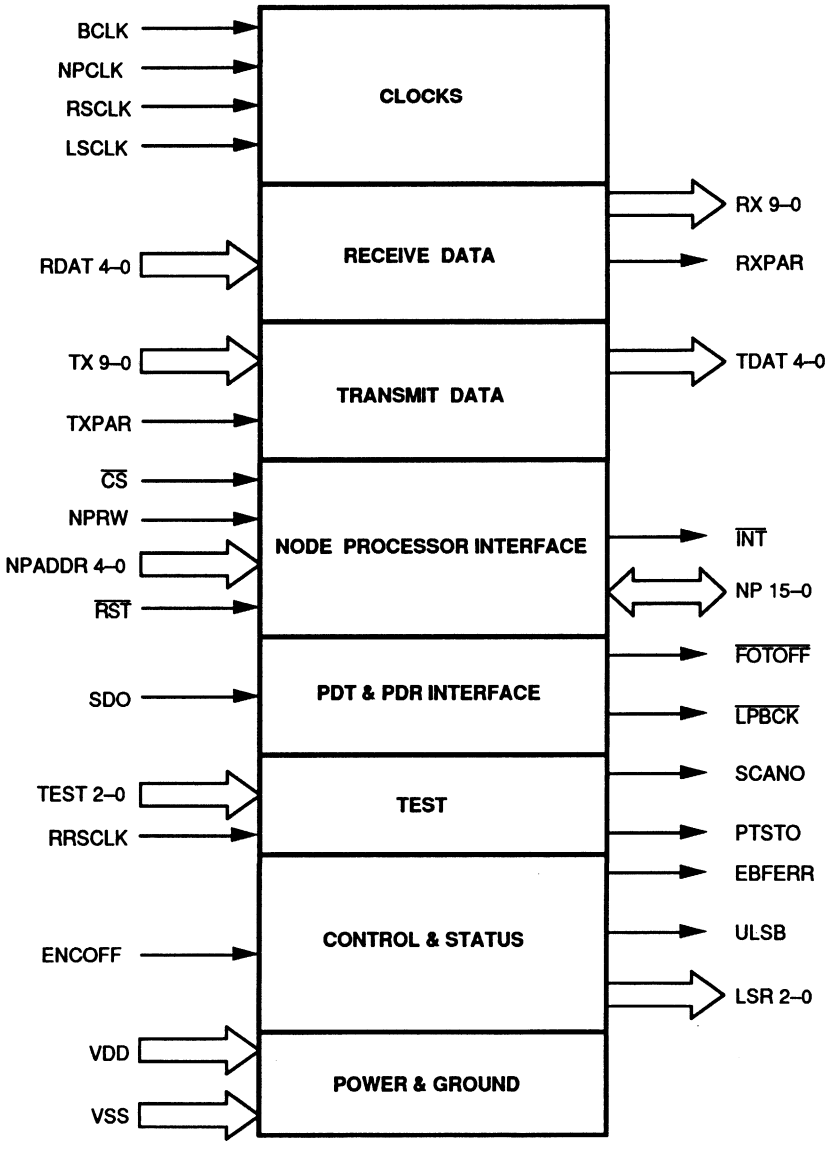


15535-003A

PQFP PIN DESIGNATIONS
Listed by pin number

Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number
VSS	1	VSS	31	VSS	61	VSS	91
$\overline{INT}$	2	EBFERR	32	RXPAR	62	VSS	92
NPADDR4	3	TEST2	33	RX0	63	$\overline{RST}$	93
NPADDR3	4	TEST1	34	RX1	64	NP0	94
NPADDR2	5	TEST0	35	RX2	65	NP1	95
NPADDR1	6	SCANO	36	RX3	66	NP2	96
VDD	7	VDD	37	VDD	67	VDD	97
VSS	8	VSS	38	VSS	68	VSS	98
NPADDR0	9	VSS	39	RX4	69	NP3	99
TDAT0	10	VSS	40	RX5	70	NP4	100
TDAT1	11	VSS	41	RX6	71	NP5	101
TDAT2	12	VSS	42	RX7	72	NP6	102
TDAT3	13	NPCLK	43	RX8	73	NP7	103
TDAT4	14	BCLK	44	RX9	74	NP8	104
VDD	15	VDD	45	VDD	75	VDD	105
VSS	16	VSS	46	VSS	76	VSS	106
$\overline{LPBCK}$	17	LSCLK	47	TX9	77	VSS	107
$\overline{FOTOFF}$	18	VSS	48	TX8	78	VSS	108
RRSCLK	19	VSS	49	TX7	79	NP9	109
RSCLK	20	PTSTO	50	TX6	80	NP10	110
RDAT4	21	ENCOFF	51	TX5	81	NP11	111
RDAT3	22	LSR2	52	TX4	82	NP12	112
VDD	23	VDD	53	VDD	83	VDD	113
VSS	24	VSS	54	VSS	84	VSS	114
RDAT2	25	LSR1	55	TX3	85	NP13	115
RDAT1	26	LSR0	56	TX2	86	NP14	116
VSS	27	VSS	57	TX1	87	NP15	117
RDAT0	28	ULSB	58	TX0	88	NPRW	118
SDO	29	VSS	59	TXPAR	89	$\overline{CS}$	119
VDD	30	VDD	60	VDD	90	VDD	120

LOGIC SYMBOL



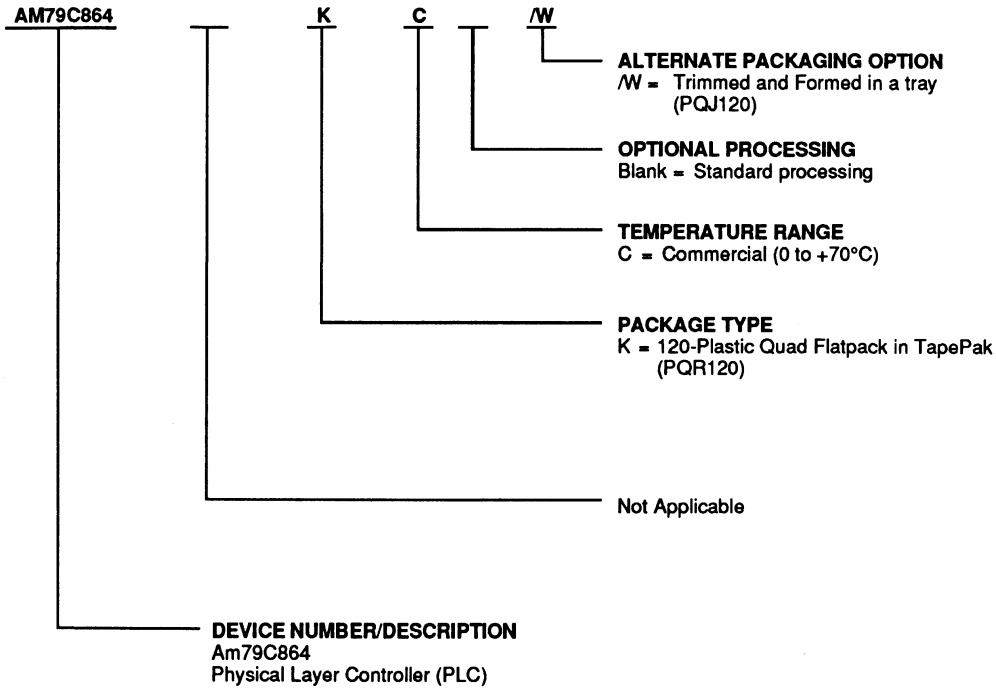
15535-004A

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

Device Number
Speed Option (if applicable)
Package Type
Temperature Range
Optional Processing
Alternate Packaging Option



Valid Combinations	
AM79C864	KC, KC/W

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

PIN DESCRIPTION

Clock Signals

BCLK

Byte Clock (Input)

BCLK is a 12.5 MHz clock. It is used by the PLC to clock most internal operations, clock RX 9–0 to the MAC device and, along with LSCLK, latch TX 9–0 from the MAC device.

NPCLK

Node Processor Clock (Input)

NPCLK is used to latch Node Processor inputs, run the Node Processor Interface state machine, and clock output signals to the Node Processor. It is distinct from the BCLK for test and diagnostic purposes only. For normal operations, the BCLK and NPCLK pins MUST be tied together.

RSCLK

Recovered Symbol Clock (Input)

RSCLK is a 25 MHz clock. It is recovered from the data sent to the Physical Data Receiver (PDR) by the upstream station in the ring. It is used to latch RDAT 4–0 from the PDR device. It is also used for clocking the Framer and the Elasticity Buffer input controller.

LSCLK

Local Symbol Clock (Input)

LSCLK is a 25 MHz clock. It is used by the PLC to clock TDAT 4–0 to the Physical Data Transmitter (PDT) and, along with BCLK, to latch TX 9–0 from the MAC device.

Receive Data Signals

RX 9–0

Receive Data Bus (Output)

RX 9–0 is a ten bit output bus used to transfer symbol pairs from the PLC to a MAC device, or to another PLC. The ten bits are clocked to the MAC device on the rising edge of BCLK. RX 9–5 contain the most significant symbol and RX 4–0 contain the least significant symbol of the framed byte. Bit 9 is the upper control bit and bit 4 is the lower control bit.

RXPAR

Receive Data Parity bit (Output)

RXPAR is an output signal used to enhance error detection on the RX bus. If there is an odd number of ones on RX 9–0 then RXPAR will be one, and if there is an even number of ones on RX 9–0 then RXPAR will be zero (even parity). When the PLC is in Bypass mode (that is when the data output on RX 9–0 is the data input on TX 9–0) RXPAR is not calculated and is just the value input on TXPAR.

RDAT 4–0

Receive Data Bus (Input)

RDAT 4–0 is a five bit input bus used to transfer data from the PDR device to the PLC. Data is latched by the PLC on the rising edge of RSCLK.

Transmit Data Signals

TDAT 4–0

Physical Transmit Data Bus (Output)

TDAT 4–0 is a five bit output bus used to transfer symbols from the PLC to the PDT. The symbols are clocked to the PDT on the rising edge of LSCLK.

TX 9–0

Transmit Data Bus (Input)

TX 9–0 is a ten bit input bus used to transfer symbol pairs from a MAC device, or from another PLC, to the PLC. The ten bits are latched by the PLC on the falling edge of LSCLK. Bits 9–5 of the bus contain the first symbol to be transmitted on the fiber and bits 4–0 contain the second symbol. Bit 9 is the upper control bit and bit 4 is the lower control bit.

TXPAR

Transmit Data Parity bit (Input)

TXPAR is an input signal used to implement even parity on the TX bus. If there is an odd number of ones on TX 9–0 then TXPAR should be one and if there is an even number of ones on TX 9–0 then TXPAR should be zero.

Node Processor Interface Signals

$\overline{\text{INT}}$

Interrupt (Output, Active Low)

The $\overline{\text{INT}}$ signal indicates an interrupt request from the PLC. This signal is active until cleared by reading the INTR_EVENT register at address 17 (hex).

$\overline{\text{CS}}$

Chip Select (Input, Active Low)

$\overline{\text{CS}}$ selects the PLC for the current bus cycle.

NPADDR 4–0

Node Processor Address Bus (Input)

The NPADDR 4–0 bus is a five bit input bus used to select one of the registers in the PLC for a read or write cycle.

NP 15–0

Node Processor Data Bus (Input/Output, Three State)

The NP 15–0 bus is a sixteen bit bi-directional, three-state data bus used to exchange data between the PLC and the Node Processor.

NPRW

Node Processor Read/Write (Input)

The NPRW signal indicates whether the current bus cycle is a read (NPRW = 1) or a write (NPRW = 0) cycle.

$\overline{RST}$

Reset (Input, Active Low, Asychronous)

The $\overline{RST}$ signal provides a means of initializing the PLC on power up. When asserted, the Reset causes the following:

- The various state machines are initialized: LSM-NOT ACTIVE, PCM-OFF, PCI-REMOVED, Repeat Filter on REPEAT, Node Processor Interface-NOT ACTIVE.
- All writeable registers are cleared and all registers that are cleared on a read are cleared.
- Built-in Self Test – OFF
- The Fiber Optic Transmitter Off ($\overline{FOTOFF}$) signal is asserted, Quiet Symbols are transmitted on TDAT, and TX is looped back onto RX.

Once $\overline{RST}$ is asserted low, it must remain asserted for at least twenty NPCLK cycles. When it is deasserted the PLC is ready to begin its normal operation.

Assertion and deassertion are asynchronous. A warm reset (assertion of $\overline{RST}$ after the device is in operation) will cause device outputs to be unpredictable until the device is initialized.

PDT and PDR Interface Signals

$\overline{LPBCK}$

Loopback (Output, Active Low)

The $\overline{LPBCK}$ signal controls the receive multiplexer in the PDR device. If LPBCK= 0, the MUX selects its input from the PDT. If LPBCK = 1, the MUX selects its input from the Fiber Optic Receiver.

$\overline{FOTOFF}$

Fiber Optic Transmitter Off (Output, Active Low)

The $\overline{FOTOFF}$ signal, when asserted, causes the PDT to transmit Quiet symbols. This signal is asserted whenever:

- The FOT_OFF bit, CD_LOOP_CNTRL bit, EB_LOC_LOOP bit, or LM_LOC_LOOP bit is set in the PLC_CNTRL_A register.
- The MAINT_LS field in the PLC_CNTRL_B register equal Transmit QUIET and the PCM is in the MAINT state.
- The Physical Connection Management logic has set LS_REQUEST = Transmit QUIET Line State.
- Built-in Self Test is active.

SDO

Signal Detect (Input, Active High)

The SDO signal is output by the PDR to indicate whether the Fiber Optic Receiver is detecting an optical signal above its threshold. The value of this signal is held in the PLC_STATUS_A register, and the LSDO interrupt bit is set whenever SDO becomes deasserted.

Test Signals

PTSTO

Parametric Test Output (Output)

This is an internal parametric test output signal. This pin should be left unconnected.

SCANO

Scan Output (Output)

The SCANO signal is used as an output of the scan chain when the PLC is in Boundary Scan Serial Test Mode.

TEST 2–0

PLC Test Mode (Input)

The three TEST 2–0 input pins are used to select between normal operating mode and three different test modes. The different operating modes are as follows:

TEST 2–0	Mode of Device Operation
0 0 0	Normal Operating Mode
0 1 X	Normal Operating Mode
0 0 1	Factory Test Mode (Counter Segmentation Test)
1 0 Scan Input	Boundary Scan Serial Test Mode
1 1 0	Boundary Scan Parallel Test Mode
1 1 1	All output pins except PTSTO are High Impedance

RRSCLK

Reserved (Input)

This pin should be connected to VSS.

Control and Status Signals

EBFERR

Elasticity Buffer Error (Output, Active High)

EBFERR indicates when an overflow or underflow condition occurs in the Elasticity Buffer.

ENCOFF

Encoder Off (Input, Active High)

The ENCOFF signal turns off the encoding function of the PLC. This allows for the transmission of any symbol, including invalid symbols for diagnostic purposes.

LSR 2–0

Line State Register (Output)

The LSR 2–0 signals directly output the LINE_ST field of the PLC_STATUS_A register to ring test and monitor equipment.

LSR 2–0	Description
000	Noise Line State (NLS)
001	Active Line State (ALS)
010	Undefined
011	Idle Line State (ILS4 – achieved after 4 Idle symbols)
100	Quiet Line State (QLS)
101	Master Line State (MLS)
110	Halt Line State (HLS)
111	Idle Line State (ILS16 – achieved after 16 Idle symbols)

ULSB

Unknown Line State (Output)

The ULSB signal directly outputs the UNKN_LINE_ST bit of the PLC_STATUS_A register to ring test and monitor equipment.

Power & Ground

VDD

Power (Inputs)

The VDD pins supply +5 V to the device.

VSS

Ground (Input)

The VSS pins ground the device.

FUNCTIONAL DESCRIPTION

Node Processor Interface (NPI)

The Node Processor Interface serves as the interface between an external Node Processor and the PLC. The interface is a general purpose synchronous interface.

The Node Processor Interface is controlled by the NPCLK. In normal operation this clock is tied to the BCLK. All signals of the NPI must be synchronous with the NPCLK, that is the signals must be stable a setup time before and a hold time after a rising edge of the NPCLK (see Figures 1, 2 and 3 and Switching Characteristics for the definition and value of all timing parameters. Figure 4 illustrates the NPI state machine).

Read Cycle

A read cycle is used by the Node Processor to read data from a PLC register. Normally the PLC is unaffected by a read, although the INTR_EVENT, VIOL_SYM_CTR, MIN_IDLE_CTR, and LINK_ERR_CTR registers are cleared when read.

A read cycle of one of the PLC registers is initiated by the assertion of the $\overline{CS}$ signal which is sampled by the rising edge of NPCLK. Once the $\overline{CS}$ signal is asserted the NPADDR bus and NPRW signals are sampled. The NPRW signal should be high for a read and low for a write. At least one half NPCLK cycle after this edge, the PLC will begin to drive the NP bus to allow the chip driving the bus in the previous read or write cycle time to tri-state the NP bus.

After the next rising edge of NPCLK (the second rising edge after the assertion of $\overline{CS}$) the data on the NP bus will be valid. It will remain valid until the second rising edge of NPCLK after the deassertion of $\overline{CS}$. The PLC will tri-state the NP bus within 1/2 NPCLK cycle after this clock edge (see Figure 1).

The timing described above will allow a read cycle every 2 NPCLK periods. However, if the Node Processor needs to extend the read cycle and have the NP bus valid longer than one clock cycle, it can delay the deassertion of the $\overline{CS}$ signal. For a minimum length read cycle (2 NPCLK periods), the Node Processor must deassert $\overline{CS}$ before the second rising edge of NPCLK following the assertion of $\overline{CS}$. If $\overline{CS}$ remains asserted after the second rising edge of NPCLK, again with respect to $\overline{CS}$ being asserted, the PLC will continue to drive the NP bus with valid data for two more rising edges of the NPCLK. By maintaining the assertion of $\overline{CS}$ beyond the initial read cycle, the read cycle will extend by two NPCLK periods (see Figure 1). The $\overline{CS}$ signal is sampled on the second and each subsequent rising edge of NPCLK after the initial assertion of $\overline{CS}$. The Node Processor can indefinitely extend the read cycle by maintaining the assertion of the $\overline{CS}$ signal. The Node Processor must deassert and then assert the $\overline{CS}$ signal for each unique read access (see Figure 1).

Write Cycle

A write cycle is used by the Node Processor to write data into a PLC control register. The Node Processor is normally allowed to write to any read-write or write-only register at any time except to the following registers XMIT_VECTOR, VECTOR_LENGTH, TPC_LOAD_VALUE, and TNE_LOAD_VALUE due to special operating conditions imposed by the PLC in their usage. If the Node Processor attempts a write on a read-only register or the special registers mentioned above at a wrong time, the PLC sets the NP_ERR bit in the INTR EVENT register. The PLC will not modify the contents of the register accessed.

The write cycle is very similar to the read cycle. The principal differences are as follows:

a) the NPRW signal must be low while $\overline{CS}$ is asserted, and

b) the data to be written must be valid on the second rising edge of NPCLK after $\overline{CS}$ is asserted (see Figure 2).

The Node Processor must tri-state the NP bus within one half NPCLK period after the second rising edge after the assertion of $\overline{CS}$. Thus, by delaying the deassertion of the $\overline{CS}$ signal, the Node Processor can extend the write cycle and the time it has to tri-state the NP bus (see Figure 2). The deassertion of the $\overline{CS}$ signal has no effect on the PLC during a write cycle. The PLC will not attempt to write to a selected register more than once until the $\overline{CS}$ signal has been deasserted. Thus, to accomplish back to back writes, the Node Processor must deassert the $\overline{CS}$ signal before attempting the second write (see Figure 2).

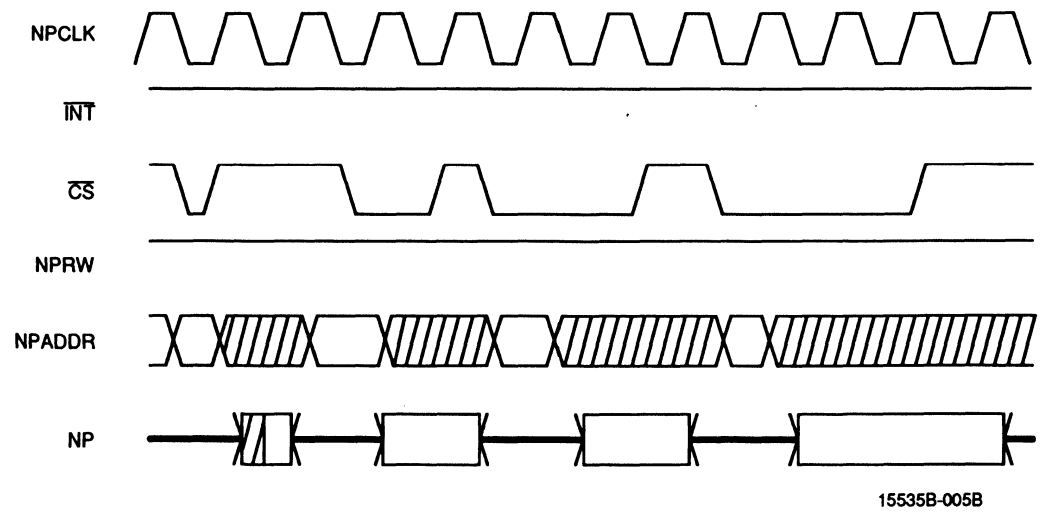


Figure 1. NP Normal and Extended Read Access

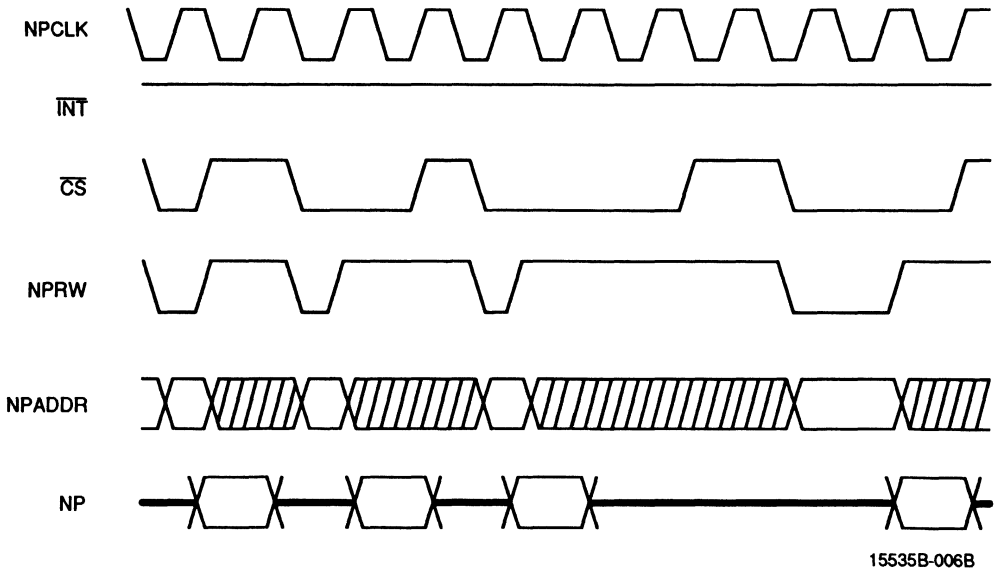


Figure 2. NP Normal and Extended Write Access

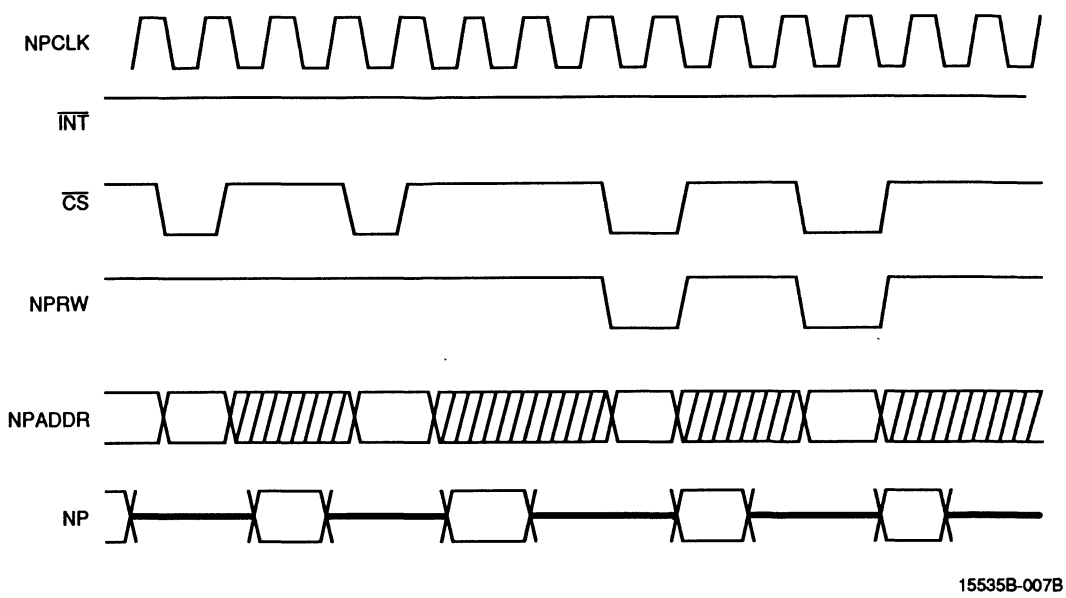


Figure 3. NP Read and Write Access

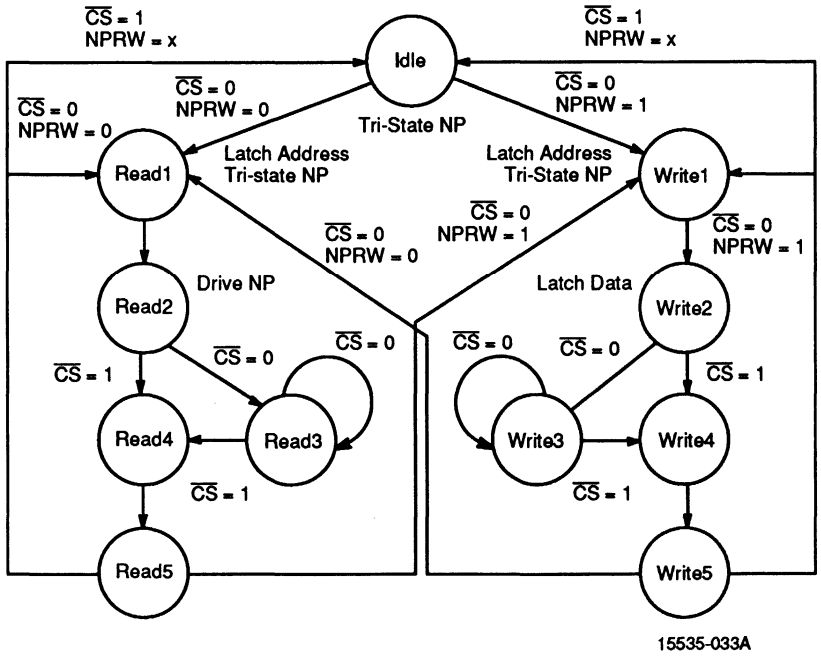


Figure 4. Node Processor Interface State Machine

Registers

The PLC contains twenty-six 16 bit registers addressed from 00 to 1A (hex). These registers are listed in Table 1.

Table 1. PLC Registers

Address (hex)	Name	Type
00	PLC_CNTRL_A	read/write
01	PLC_CNTRL_B	read/write
02	INTR_MASK	read/write
03	XMIT_VECTOR	read/write (Note 1)
04	VECTOR_LENGTH	read/write (Note 1)
05	LE_THRESHOLD	read/write
06	C_MIN	read/write
07	TL_MIN	read/write
08	TB_MIN	read/write
09	T_OUT	read/write
0B	LC_LENGTH	read/write
0C	T_SCRUB	read/write
0D	NS_MAX	read/write
0E	TPC_LOAD_VALUE	write only (Note 2)
0F	TNE_LOAD_VALUE	write only (Note 3)
10	PLC_STATUS_A	read only
11	PLC_STATUS_B	read only
12	TPC	read only
13	TNE	read only
14	CLK_DIV	read only
15	BIST_SIGNATURE	read only
16	RCV_VECTOR	read only
17	INTR_EVENT	read only (Note 4)
18	VIOL_SYM_CTR	read only (Note 4)
19	MIN_IDLE_CTR	read only (Note 4)
1A	LINK_ERR_CTR	read only (Note 4)

Notes:

1. Writeable only when the PCM_SIGNALING bit in the PLC_STATUS_B register is not set.
2. Writeable only when the PCM is in the MAINT state.
3. Writeable only when the PCM is in the MAINT state and the NOISE_TIMER bit in the PLC_CONTROL_A register is not set.
4. Register cleared on read.

PLC Control and Status Registers

The control and status information for the PLC is contained in four registers.

PLC Control Register A (PLC_CNTRL_A)

PLC_CNTRL_A has address 00 (hex). It is readable and writeable. All bits of this register are cleared with the assertion of $\overline{RST}$. PLC_CNTRL_A is used for the following functions:

- Timer configuration
- Specification of PCM MAINT state options
- Counter interrupt frequency
- PLC data path configuration
- Execution of PLC Built In Self Test

Note that several bits of this register can only be written if the PCM is in the OFF or MAINT state. If this register is written when the PCM is in any other state these bits will remain unchanged.

The PLC_CNTRL_A register bit assignments are listed in Table 2.

Addr (Hex) PLC_CNTRL_A

00	-	NOISE TIMER	TNE-16 BIT	TPC-16 BIT	REQ-SCRUB	-	VSYM--CTR-INTRS	MINI-CTR-INTRS	LOOP BACK	FOT-OFF	EB-LOC-LOOP	LM-LOC-LOOP	SC-BYPASS	SC-REM-LOOP	RF-DISABLE	RUN-BIST
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

15535-008A

Table 2. PLC_CNTRL_A

Bit	Name	Definition
15		Reserved
14	NOISE_TIMER	The NOISE_TIMER bit allows the noise timing function of the PCM to be used when the PCM is in the MAINT state. This function causes the TNE Timer to be loaded with the value in the NS_MAX register whenever the Line State Machine transitions from Idle Line State to Noise Line State, Active Line State or Unknown Line State. If the timer expires before Idle Line State is recognized, the TNE_EXPIRED bit in the INTR_EVENT register is set.
13	TNE_16BIT	When TNE_16BIT is set it causes the TNE Timer to operate as a 16 bit timer. In this mode the 2 bits of the TNE Clock Divider are bypassed and the TNE Timer is incremented every 80 nanoseconds. TNE_16BIT can only be written if the PCM is in the OFF or MAINT state.
12	TPC_16BIT	When TPC_16BIT is set it causes the TPC Timer to operate as a 16 bit timer. In this mode the 8 bits of the TPC Clock Divider are bypassed and the TPC Timer is incremented every 80 nanoseconds. TPC_16BIT can only be written if the PCM is in the OFF or MAINT state.
11	REQ_SCRUB	The REQ_SCRUB bit allows limited access to the scrub capability of the PLC chip. If the PCM is in the MAINT state or if the CONFIG_CNTRL bit in the PLC_CNTRL_B register is set then the REQ_ SCRUB bit controls the Scrub MUX. If REQ_SCRUB is set then Idle symbols are sourced at the RX 9–0 output port. The output at the TDAT 4–0 output port is controlled separately by the MAINT_LS field in the PLC_CNTRL_B register. This bit may be written at any time, but only takes effect when the PCM is in the MAINT state or if the CONFIG_CNTRL bit in the PLC_CNTRL_B register is set.
10		Reserved
09	VSYM_CTR_INTRS	The VSYM_CTR_INTRS bit controls when the VSYM_CTR interrupt bit in the INTR_EVENT register is asserted. When VSYM_CTR_INTRS is set the interrupt is generated only when the VIOL_SYM_CTR overflows (reaches 256). When VSYM_CTR_INTRS is cleared, the interrupt is generated every time the VIOL_SYM_CTR is incremented (whenever a violation symbol is detected).
08	MINI_CTR_INTRS	The MINI_CTR_INTRS bit partially controls when the MINI_CTR interrupt bit in the INTR_EVENT register is asserted. When MINI_CTR_INTRS is set the interrupt is generated when the Minimum Idle Gap Counter portion of MIN_IDLE_CTR overflows (reaches16). When MINI_CTR_INTRS is cleared the interrupt is generated every time the counter is incremented (whenever a minimum length Idle gap is detected). Note that this bit does not affect interrupts caused by the Idle Counter Minimum Detector portion of MIN_IDLE_CTR.
07	LOOPBACK	When LOOPBACK is set it causes the $\overline{\text{LPBCK}}$ output pin to be asserted low. This, in turn, causes data to be looped back from the output of the PDT chip to the input of the PDR chip.

Table 2. PLC_CNTRL_A (Continued)

Bit	Name	Definition
06	FOT_OFF	The setting of this bit will cause the assertion of the $\overline{\text{FOTOFF}}$ output pin of the PLC.
05	EB_LOC_LOOP	When EB_LOC_LOOP is set a loopback path is set up in the PLC chip just prior to the PLC to PDT/PDR interface. Data from the PLC transit path are looped back to the input of the Framer. This loopback path is also set up when the PLC is executing its Built In Self Test. Note that this bit also controls which clock the Framer and Elasticity Buffer use. When it is not set the Recovered Byte Clock is derived from the RSCLK input pin, and when it is set the BCLK is used. Thus, when this bit gets set a clock glitch could be created which could cause receive data to be indeterminate for a clock cycle, spurious interrupts, and unknown values in the event counters. EB_LOC_LOOP can only be written if the PCM is in the OFF or MAINT state.
04	LM_LOC_LOOP	When LM_LOC_LOOP is set a loopback path is set up in the PLC chip such that data from TX 9–0 are passed through the PLC transmit path and looped back to the input of the receive path just after the Elasticity Buffer at the LM Local Loopback MUX. This loopback path differs from EB_LOC_LOOP in that the Framer and Elasticity Buffer are bypassed. LM_LOC_LOOP can only be written if the PCM is in the OFF or MAINT state.
03	SC_BYPASS	The SC_BYPASS bit provides limited control over the PLC's data path by providing a physical bypass of the PLC. If the PCM is in the MAINT state or if the CONFIG_CNTRL bit in the PLC_CNTRL_B register is set then the SC_BYPASS bit controls the Bypass MUX. If both SC_BYPASS and REQ_ SCRUB are asserted then RX 9–0 is driven with Idle symbols. If SC_BYPASS is asserted and REQ_SCRUB cleared then RX 9–0 is driven by the data entering the PLC at the TX 9–0 input. Otherwise, RX 9–0 is driven by the data entering the PLC at the RDAT 4–0 input. This bit may be written at any time, but only takes effect when the PCM is in its MAINT state or if the CONFIG_CNTRL bit in the PLC_CNTRL_B register is set.
		SC_BYPASS / **REQ_SCRUB** / **RX 9–0** SET / SET / IDLE SET / RESET / TX 9–0 RESET / RESET / RDAT 4–0 RESET / SET / RDAT 4–0
02	SC_REM_LOOP	When SC_REM_LOOP is set a remote loopback path is set up inside the PLC where symbols from the receive data path are looped back onto the transmit data path, traversing all of both paths except for the receive data output latch and the transmit data input latch. If the PCM is in the MAINT state or if the CONFIG_CNTRL bit in the PLC_CNTRL_B register is set then the SC_REM_LOOP bit controls the Remote Loopback MUX. This loopback is used by the PCM to control the configuration and can be used to monitor the ring or otherwise control configuration during normal operation. This bit only has effect if the EB_LOC_LOOP and LM_LOC_LOOP bits are not asserted. This bit may be written at any time, but only takes effect when the PCM is in the MAINT state or if the CONFIG_CNTRL bit in the PLC_CNTRL_B register is set.
01	RF_DISABLE	When RF_DISABLE is set it disables the Repeat Filter state machine in the PLC.
00	RUN_BIST	When RUN_BIST is set it causes the PLC to begin running its Built In Self Test. The completion of BIST is indicated via an interrupt. BIST can be stopped before completion by clearing this bit. Once BIST has completed, this bit must be cleared and set again before BIST will restart. For more detail, refer to page 29 and 42.

PLC Control Register B (PLC_CNTRL_B)

PLC_CNTRL_B has address 01 (hex). It is readable and writeable. All bits of this register are cleared with the assertion of $\overline{RST}$. PLC_CNTRL_B contains signals and requests to direct the process of physical connection management. It is also used to control the Line State Match interrupt.

The PLC_CNTRL_B register bit assignments are listed in Table 3.

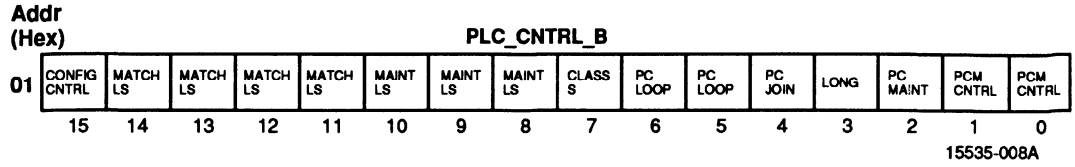


Table 3. PLC_CNTRL_B

Bit	Name	Definition
15	CONFIG_CNTRL	The CONFIG_CNTRL bit allows control over the Scrub, Bypass, and Remote Loopback datapath MUXes while the PCM is in normal operation. If this bit is set then the REQ_SCRUB, SC_BYPASS, and SC_REM_LOOP bits in the PLC_CNTRL_A register will have effect regardless of the state of the PCM. If this bit is not set then the REQ_SCRUB, SC_BYPASS and SC_REM_LOOP bits will only have effect if the PCM is in the MAINT state.
14–11	MATCH_LS	The MATCH_LS field specifies line states to be compared with the currently detected line state (as defined by LINE_ST in the PLC_STATUS_A register). When a match occurs the LS_MATCH interrupt bit in the INTR_EVENT register is asserted. Each bit of MATCH_LS corresponds to a line state. If more than one bit is set the interrupt is signalled if any of the line states match the current line state. If no bits are set the interrupt is signalled on any change in the LINE_ST field or the UNKN_LINE_ST bit. It is defined as follows:
		MATCH_LS — **Description** 0000 — Interrupt on any change in LINE_ST or UNKN_LINE_ST 1XXX — Interrupt on Quiet Line State X1XX — Interrupt on Master Line State XX1X — Interrupt on Halt Line State XXX1 — Interrupt on Idle Line State
		In the above table "X" means don't care. Also Idle Line State refers to ILS16, which is signalled only after sixteen Idle symbols (eight Idle bytes) have been received.
10–8	MAINT_LS	The MAINT_LS field defines the line state the PCM will source while in the MAINT state. The PCM enters the MAINT state from the OFF state if the PC_MAINT bit is asserted. It is further defined as follows:
		MAINT_LS — **Description** 000 — Transmit QUIET Line State 001 — Transmit IDLE Line State 010 — Transmit HALT Line State 011 — Transmit MASTER Line State 100 — Transmit QUIET Line State 101 — Transmit QUIET Line State 110 — Transmit PDR (Transmit PHY_DATA request)—the symbol stream at TX 9–0 is transmitted 111 — Transmit QUIET Line State

Table 3. PLC_CNTRL_B (Continued)

Bit	Name	Definition
07	CLASS_S	When CLASS_S is set, signifying that the PHY is a single attach station, the station will not be bypassed before the PCM gets to the ACTIVE state. Note that this bit has effect when the PCM is in normal operation. When the PCM is in the MAINT state the REQ_SCRUB and SC_BYPASS bits in the PLC_CNTRL_A register control the bypass operation. This bit can only be changed when the PCM is in the OFF state. If this bit is written when the PCM is in any other state, the change will be ignored.
06–05	PC_LOOP	PC_LOOP controls the loopback used in the Link Confidence Test (LCT). When it is set to a value other than zero and the PCM is in the NEXT state, the PCM will perform the LCT in one of three ways. The following table describes the action taken according to the value of the two bits:
		PC_LOOP / **Description** 00 — No LCT is performed 01 — The PCM asserts Transmit PDR. This assumes that Protocol Data Units (PDUs) will be input at TX(9–0). 10 — The PCM asserts Transmit Idle. This causes the PLC to source Idle symbols. 11 — The PCM asserts Transmit PDR and sets up a remote loopback path in the PLC.
		PC_LOOP should only be written after the PCM_CODE interrupt has been generated. If the PCM is not in the NEXT state, or if PCM_SIGNALING is set, then any value written to this field will be ignored. Once PC_LOOP has been written, it must be cleared and then written again to perform another LCT.
04	PC_JOIN	When PC_JOIN is set and the PCM is in the NEXT state the PCM will transition to the JOIN state and the PCM join sequence will be started. PC_JOIN should only be written after the PCM_CODE interrupt has been generated. If the PCM is not in the NEXT state, or if PCM_SIGNALING is set, then any value written to this field will be ignored. After this bit is set it must be cleared and then set again to cause another transition from the NEXT state to the JOIN state. Note that if PC_JOIN is set after the LCT has been started but before it has completed then the LCT will be aborted and the PCM join sequence started.
03	LONG	When LONG is set the PCM will perform a long LCT, that is, it will continue the test until the processor issues a PC_SIGNAL, PC_JOIN, or other command. Otherwise it will perform a LCT, that is, it will stop the test after the length of time indicated in the LC_LENGTH register. In either case LCT will stop whenever Master Line State or Halt Line State is detected, indicating that the neighboring station has completed its LCT and has started signaling.
02	PC_MAINT	When PC_MAINT is set the PCM state machine transitions to the MAINT state if it is currently in the OFF state. If the PCM is not in the OFF state when this bit is written, and subsequently transitions to the OFF state, it will immediately transition to the MAINT state.

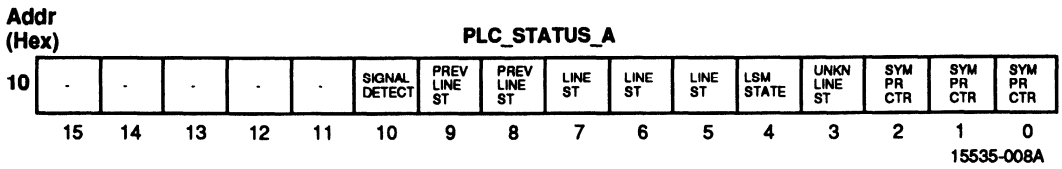
Table 3. PLC_CNTRL_B (Continued)

<table>
<tr><th>Bit</th><th>Name</th><th>Definition</th></tr>
<tr><td>01–00</td><td>PCM_CNTRL</td><td>PCM_CNTRL controls the PCM state machine. When set to a value other than zero it will cause the PCM to immediately make a transition to the BREAK, TRACE or OFF state. The transition to the BREAK or OFF state will occur regardless of the state the PCM is in at the time. The transition to the TRACE state will only be made if the PCM is in the ACTIVE state, otherwise PCM_CNTRL will be ignored. The following table describes the action taken according to the value of the two bits:
<table>
<tr><th>PCM_CNTRL</th><th>Description</th></tr>
<tr><td>00</td><td>The PCM state is not affected</td></tr>
<tr><td>01</td><td>The PCM goes to the BREAK state (PC_Start)</td></tr>
<tr><td>10</td><td>The PCM goes to the TRACE state (PC_Trace)</td></tr>
<tr><td>11</td><td>The PCM goes to the OFF state (PC_Stop)</td></tr>
</table>
After a PC_Start (PCM_CNTRL=01) has been issued and before another one can be issued, PCM_CNTRL must first be written with zero and then written with the PC_Start value again. Note that if the PCM goes to the BREAK state for a reason other than writing PCM_CNTRL (e.g. QLS is received, or a timeout occurs), then the PCM will not go to the CONNECT state and will remain in the BREAK state until PCM_CNTRL is written with the PC_Start value. If the PCI is in the INSERTED state when PC_Start or PC_Stop is issued then scrubbing will be performed. If the PCI is in the INSERT_SCRUB or REMOVE_SCRUB state when PC_Start or PC_Stop is issued the scrubbing will be completed before the PCM enters the BREAK or OFF state.</td></tr>
</table>

PLC Status Register A (PLC_STATUS_A)

PLC_STATUS_A has address 10 (hex). It is read-only. It is used to report status information to the Node Processor about the Line State Machine (LSM).

The PLC_STATUS_A register bit assignments are listed in Table 4.



15535-008A

Table 4. PLC_STATUS_A

Bit	Name	Definition	
15–11		Reserved	
10	SIGNAL_DETECT	This bit, when set, indicates that signal detect is deasserted. If SDO equals zero then SIGNAL_DETECT is one, if SDO equals one then SIGNAL_DETECT is zero.	
09–08	PREV_LINE_ST	This field contains the value of the previous line state whenever line state changes from Quiet Line State, Master Line State, Halt Line State or Idle Line State (ILS16, where ILS16 is achieved after 16 idle symbols) to another line state. When the line state changes from anything else this field will not be updated. It is further defined as follows:	
		PREV_LINE_ST	**Description**
		00	Quiet Line State (QLS)
		01	Master Line State (MLS)
		10	Halt Line State (HLS)
		11	Idle Line State (ILS16 – achieved after 16 idle symbols)
07–05	LINE_ST	This field contains the most recently recognized Line State by the LSM. LINE_ST is further defined as follows:	
		LINE_ST	**Description**
		000	Noise Line State (NLS)
		001	Active Line State (ALS)
		010	Undefined
		011	Idle Line State (ILS4 – achieved after 4 Idle symbols)
		100	Quiet Line State (QLS)
		101	Master Line State (MLS)
		110	Halt Line State (HLS)
		111	Idle Line State (ILS16 – achieved after 16 Idle symbols)
04	LSM_STATE	This field contains the state bit of the LSM state machine.	
03	UNKN_LINE_ST	This bit is the Unknown Line State Bit from the LSM. Since a minimum of sixteen symbols is required to satisfy the entry conditions of a line state (four symbols in the case of Idle Line State), the LSM uses this bit to indicate it is attempting to recognize a new line state. This bit is set to a one when the line state is unknown and reset to a zero when known.	
02–00	SYM_PR_CTR	This field contains the LSM Symbol Pair Counter. When the count reaches seven, indicating eight consecutive like symbol pairs, then Current Line State is set with the new line state and the Unknown Line State Bit is reset. Note that Idle Line State (ILS4) is reached after just two Idle symbol pairs.	

PLC Status Register B (PLC_STATUS_B)

PLC_STATUS_B has address 11 (hex). It is read-only. It contains signals and status from the Repeat Filter and Physical Connection Management state machine (PCM).

The PLC_STATUS_B register bit assignments are listed in Table 5.

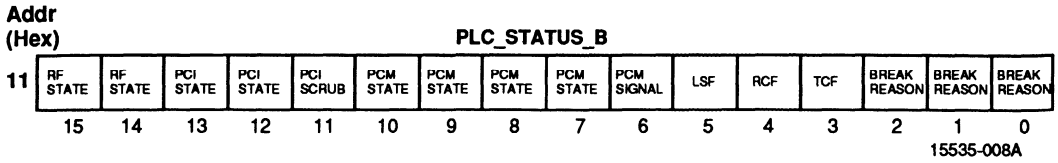


Table 5. PLC_STATUS_B

Bit	Name	Definition	
15–14	RF_STATE	This field contains the state bits of the Repeat Filter state machine. The states are defined as follows:	
		RF_STATE	**Name**
		00	REPEAT
		01	IDLE
		10	HALT1
		11	HALT2
13–12	PCI_STATE	This field contains the state bits of the Physical Connection Insertion state machine. The states are defined as follows:	
		PCI_STATE	**Name**
		00	REMOVED
		01	INSERT_SCRUB
		10	REMOVE_SCRUB
		11	INSERTED
11	PCI_SCRUB	The PCI_SCRUB flag indicates that the scrubbing function is being executed, that is Idle symbol pairs are being sourced on the RX output pins.	
10–07	PCM_STATE	This field contains the state bits of the Physical Connection Management state machine. The states are defined as follows:	
		PCM_STATE	**Name**
		0000	PC0 (OFF)
		0001	PC1 (BREAK)
		0010	PC2 (TRACE)
		0011	PC3 (CONNECT)
		0100	PC4 (NEXT)
		0101	PC5 (SIGNAL)
		0110	PC6 (JOIN)
		0111	PC7 (VERIFY)
		1000	PC8 (ACTIVE)
		1001	PC9 (MAINT)
		1010–1111	Reserved

Table 5. PLC_STATUS_B (Continued)

Bit	Name	Definition
06	PCM_SIGNALING	PCM_SIGNALING is a flag from the PCM indicating that the XMIT_VECTOR register has been written. The XMIT_VECTOR and VECTOR_LENGTH registers cannot be written when this flag is set.
05	LSF	The Line State Flag is used by the PCM to indicate that a given line state has been received since entering the current state. It is cleared on every change of PCM state.
04	RCF	The Receive Code Flag is used by the PCM to indicate that the Receive Pseudo Code has started execution. This flag is used to prevent the Receive Pseudo Code from being started multiple times while in the NEXT state.
03	TCF	The Transmit Code Flag is used by the PCM to indicate that the Transmit Pseudo Code has started execution. This flag is used to prevent the Transmit Pseudo Code from being started multiple times while in the NEXT state.
02–00	BREAK_REASON	This field indicates the reason for the PCM state machine's last transition to the BREAK state. It is defined as follows:

BREAK_REASON	Description
000	The PCM state machine has not gone to the BREAK state.
001	PC_Start issued
010	TPC Timer expired after T_OUT
011	TNE Timer expired after NS_MAX
100	Quiet Line State detected
101	Idle Line State detected
110	Halt Line State detected
111	Reserved

Physical Connection Management (PCM) Timers

The PCM contains two timers, TPC and TNE. Both timers have a clock divider circuit to reduce the fequency at which they are clocked.

TPC Timer

The TPC Timer is a 16 bit timer. In normal operation it is read-only by the Node Processor. TPC is read at address 12 (hex). When the PCM is in the MAINT state a value can be written to TPC by writing TPC_LOAD_VALUE at address 0E. The TPC Timer is incremented by the output of an 8 bit clock divider circuit. It is incremented every 20.48 microseconds (2^8 times 80 nanoseconds). The value in the TPC Clock Divider is contained in bits 7 through 0 of the CLK_DIV register at address 14 (hex).

The TPC Timer is used while the PCM is attempting to establish a physical connection with a neighboring PCM. It is used to ensure that state transitions proceed at the desired rate.

The timer is loaded with a two's complement value and counts up until it reaches zero. In normal operation the timer is loaded by the PCM from the TPC Timing Parameter Registers, which contain the two's complement of the time value in 20.48 microsecond units. At the same time the TPC Timer is loaded the TPC Clock Divider is loaded with zero.

When the PCM is in the MAINT state the TPC Timer can be loaded directly from the Node Processor. The Node Processor accomplishes this by writing a 16 bit value which is loaded into the timer (the TPC Clock Divider is loaded with zero). The value written is the two's complement of the time in 20.48 microsecond units. If the PCM is not in the MAINT state when a write is attempted to the TPC timer, the NP_ERR bit in the INTR_EVENT register will be set and the timer will not be loaded.

The timer may also be used in 16 bit mode, where the TPC Clock Divider is bypassed and the timer is incremented every 80 nanoseconds when in operation. In this mode the value loaded into the timer is the two's complement of the time remaining in 80 nanosecond units. This feature, controlled by the TPC_16BIT bit in the PLC_CNTRL_A register, is intended for test purposes, where it is desirable to run the timer for only short periods of time.

TNE Timer

The TNE Timer is a 16 bit timer. In normal operation it is read-only by the Node Processor. TNE is read at address 13 (hex). When the PCM is in the MAINT state and the NOISE_TIMER bit in the PLC_CNTRL_A register is not set a value can be written to TNE by writing TNE_LOAD_VALUE at address 0F. The TNE Timer is incremented by the output of a 2 bit clock divider circuit. It is incremented every 0.32 microseconds (2^2 times 80 nanoseconds). The value in the TNE Clock Divider is contained in bits 9 and 8 of the CLK_DIV at address 14 (hex).

The TNE Timer is used to time the length of (potential) noise events while the PCM is in the ACTIVE state. The TNE Timer is started whenever the Line State Machine transitions from Idle Line State to Noise Line State, Active Line State, or Unknown Line State. If the timer expires before the LSM recognizes Idle Line State again, the PCM transitions to the BREAK state.

The timer is loaded with a two's complement value and counts up until it reaches zero. In normal operation the timer is loaded by the PCM from the NS_MAX Timing Parameter Register, which contains the two's complement of the time value in 0.32 microsecond units, whenever the LSM leaves Idle Line State. At the same time the TNE Timer is loaded the TNE Clock Divider is loaded with zero.

When the PCM is in the MAINT state the TNE timer can be loaded directly from the Node Processor. The Node Processor accomplishes this by writing a 16 bit value which is loaded into the timer (the TNE Clock Divider is loaded with zero). The value written is the two's complement of the time in 0.32 microsecond units. If the PCM is not in the MAINT state when a write is attempted to the TNE timer, the NP_ERR bit in the INTR_EVENT register will be set and the timer will not be loaded.

Note that through use of the NOISE_TIMER bit in the PLC_CNTRL_A register the TNE Timer can be used to time noise duration when the PCM is in the MAINT state without the timer having to be explicitly loaded by the Node Processor. The Node Processor should not attempt to load the TNE Timer when the NOISE_TIMER bit in the PLC_CNTRL_A is set. If this condition is violated the NP_ERR bit in the INTR_EVENT register will be set and the timer will not be loaded.

The timer may also be used in 16 bit mode, where the TNE Clock Divider is bypassed and the timer is incremented every 80 nanoseconds when in operation. In this mode the value loaded into the timer is the two's complement of the time remaining in 80 nanosecond units. This feature, controlled by the TNE_16BIT bit in the PLC_CNTRL_A register, is intended for test purposes, where it is desirable to run the timer for only short periods of time.

Physical Connection Management Timing Parameters

The PCM uses a number of different timing parameters while forming a physical connection. The parameters are programmable and must be written by the node processor. The registers are readable at any time. The parameters are sixteen bits in length and are loaded into the TPC Timer. They hold the two's complement of the time in 20.48 microsecond (2^8 times 80 nanoseconds) units. They have a maximum value of about 1.34 seconds (2^{16} times 20.48 microseconds). When the TPC Timer is in 16 bit mode the timing parameters are the two's complement of the time in 80 nanosecond units and can have a maximum value of about 5.24 milliseconds (2^{16} times 80 nanoseconds).

In addition to the TPC Timing Parameters there is one timing parameter used by the TNE Timer. Unlike the TPC Timing Parameters, NS_MAX holds the two's complement of the time in 0.32 microsecond (2^2 times 80 nanoseconds) units. It can have a maximum value of about 20.97 milliseconds (2^{16} times 0.32 microseconds). When the TNE Timer is in 16 bit mode NS_MAX is the two's complement of the time in 80 nanosecond units and can have a maximum value of about 5.24 milliseconds (2^{16} times 80 nanoseconds).

Table 6 summarizes the PCM timing parameters.

Minimum Connect State Time Register (C_Min)

The Minimum Connect State Time (C_Min) register has address 06 (hex). It has a recommended value of 1.6 milliseconds (FFB2 hex in 2's complement). This is the minimum time required to remain in the Connect State to assure that the other end has recognized HALT Line State.

Minimum Line State Transmit Time Register (TL_Min)

The Minimum Line State Transmit Time Register (TL_Min) has address 07 (hex). It has a recommended value of 0.03 milliseconds (FFFE hex in 2's complement). This is the minimum time required to transmit a Line State before advancing to the next PCM state.

Minimum Break Time Register (TB_MIN)

The Minimum Break Time (TB_MIN) register has address 08 (hex). It has a recommended value of 5 milliseconds (FF10 hex in 2's complement). When PCM performs a break (in state BREAK), the break shall be of adequate length to allow time for a response to be seen on the inbound physical link. This time allows for the possibility of a bypass failure mode in this or a neighboring station that could cause four PHYs to be connected in a loop and produce an invalid response to the break. The minimum break time guarantees that in this case the response to the break will propagate around the loop and be seen on the inbound link.

Signaling Timeout Register (T_OUT)
The Signaling Timeout (T_OUT) register has address 09 (hex). It has a recommended value of 100 milliseconds (ECED hex in 2's complement). A response from a neighboring PCM must be received by T_OUT. When a response is expected and no transition is made in T_OUT time, a transition is made to the BREAK state.

Link Confidence Test Time Register (LC_LENGTH)
The Link Confidence Test (LCT) Time register (LC_LENGTH) has address 0B (hex). This register specifies the time duration of the LCT and limits the duration of loopback to prevent deadlock. It has a recommended value of 50 milliseconds (F676 hex in 2's complement) for the short LCT. For medium LCT, it has a recommended value of 500 ms (A0A2 hex in 2's complement).

Scrub Time Register (T_SCRUB)
The Scrub Time (T_SCRUB) register has address 0C (hex). It has a recommended value of 3.5 milliseconds. T_SCRUB is the same as the MAC TVX time. Its use is described in the Physical Connection Insertion Process functional description.

Noise Time Register (NS_MAX)
The Noise Time (NS_MAX) register has address 0D (hex). It has a recommended value of 2 milliseconds. NS_MAX is the maximum length of time that noise is tolerated before a connection is broken down.

The Table 6 summarizes the recommended values for the timing parameter registers. Also shown is the 2's complement, hexadecimal equivalent of the recommended value and the timer used for the parameter.

Table 6. Summary of PCM Timing Parameters

Parameter	Recommended Value (ms)	Register Value (2's comp/hex)	Timer	Address (hex)
C_MIN	1.6	FFB2	TPC	06
TL_MIN	0.03	FFFE	TPC	07
TB_MIN	5	FF10	TPC	08
T_OUT	100	ECED	TPC	09
LC_LENGTH	50	F676	TPC	0B
LC_LENGTH	500	A0A2	TPC	0B
T_SCRUB	3.5	FF6D	TPC	0C
NS_MAX	2	E796	TNE	0D

Physical Connection Management Bit Signaling Registers

The PLC contains three registers used by the PCM to perform bit signaling. Bit signaling is the mechanism the PCM uses to transfer information to the PCM in the neighboring station.

Transmit Vector Register (XMIT_VECTOR)
The Transmit Vector register has address 03 (hex). It is readable and writable. All bits of the register are cleared with the assertion of $\overline{RST}$. The PCM_SIGNALING bit must not be asserted in order to write to this register. If PCM_SIGNALING is asserted when a write is attempted the register will not be written and the NP_ERR bit in the INTR_EVENT register will be set. This register is readable at any time.

The Transmit Vector consists of from one to sixteen bits of data to be transmitted to the neighboring PCM. Bits are transmitted one at a time by the bit signaling mechanism. A one bit is represented by the transmission of Halt Line State and a zero bit by Master Line State. Bit 0 of this register is the first bit to be transmitted, then bit 1, etc., up to the number of bits specified in the VECTOR_LENGTH register.

Writing this register causes PCM_SIGNALING to be asserted. Therefore, the VECTOR_LENGTH register must be initialized before this register is written.

Transmit Vector Length Register (VECTOR_LENGTH)
The Transmit Vector Length register has address 04 (hex). It is readable and writable. All bits of the register are cleared with the assertion of $\overline{RST}$. The PCM_SIGNALING bit must not be asserted in order to write to this register. If PCM_SIGNALING is asserted when a write is attempted, the register will not be written and the NP_ERR bit in the INTR_EVENT register will be set. This register is readable at any time.

Bits 15 through 4 of this register are unused. Any value written to these bits will be ignored. These bits will always be read as zeros.

Bits 3 through 0 of this register contain the number of bits in the XMIT_VECTOR register to transmit. The value in this field (0 to 15) is actually one less than the number of bits to transmit (1 to 16).

Receive Vector Register (RCV_VECTOR)
The Receive Vector register has address 16 (hex). It is read only.

The Receive Vector consists of from one to sixteen bits of data received from the neighboring PCM. Bits are received at the same time bits are being transmitted. As bit n is being transmitted from the Transmit Vector, bit n is received and placed in the Receive Vector register. If Halt Line State is received, then bit n is a one, and if Master Line State is received then bit n is a zero. Bit 0 of this register is the first bit received, then bit 1, etc., up to the number of bits specified in the VECTOR_LENGTH register.

Although this register is readable at any time, if PCM_SIGNALING bit is asserted when this register is read the data may be incomplete.

Event Counters

The PLC contains three event counter registers and one threshold value register, used for gathering information about errors occurring on its associated physical link and for monitoring Idle symbol gaps between packets.

Violation Symbol Counter (VIOL_SYM_CTR)
The Violation Symbol Counter has address 18 (hex). It is read-only and is cleared whenever it is read as well as when $\overline{RST}$ is asserted. The high order 8 bits of the register will always be read as zeros. The low order 8 bits will contain the counter value. The VSYM_CTR bit in the INTR_EVENT register is set whenever the counter increments or whenever the counter overflows (reaches 256), depending on the setting of the VSYM_CTR_INTRS bit in the PLC_CNTRL_A register. When the counter overflows it wraps to zero and continues to count.

The Violation Symbol Counter is incremented whenever the 4B/5B decoder in the PLC decodes a violation symbol. See the Decoder description for the symbols considered to be violation symbols by the Decoder. They are represented as a "V" in the table 12.

Minimum Idle Counter (MIN_IDLE_CTR)
The Minimum Idle Counter has address 19 (hex). It is read-only and is cleared whenever it is read as well as when $\overline{RST}$ is asserted. The high order 9 bits of the register will always be read as zeros.

Bits 6 through 4 of the counter contain the value in the Idle Counter Minimum Detector. This is the minimum number of inter-packet Idle symbol pairs seen since the counter was last reset. It gets reset to 7. Whenever the value changes to a lower value the MINI_CTR bit in the INTR_EVENT register is set. The Idle symbol pair count definitions are given in the following table.

MIN_IDLE_CTR 6–4	Idle Symbol Pair Count
100	7 or more
101	6
111	5
110	4
010	3
011	2
001	1
000	0

Bits 3 through 0 of the counter contain the value in the Minimum Idle Gap Counter. This is the number of times the minimum number of inter-packet Idles has been seen since the last reset. It gets reset to 1. The MINI_CTR bit in the INTR_EVENT register is set whenever the counter increments or whenever the counter overflows (reaches 16), depending on the setting of the MINI_CTR_INTRS bit in the PLC_CNTRL_A register. When the counter overflows it remains at 16. The minimum Idle occurrence count definitions are given in the following table.

MIN_IDLE_CTR 3–0	Minimum Idle Occurrence Count
0000	1
1000	2
1100	3
0100	4
0101	5
0111	6
1111	7
1110	8
1010	9
0010	10
0011	11
0001	12
1001	13
1101	14
0110	15
1011	16

Link Error Event Counter (LINK_ERR_CTR)
The Link Error Event Counter has address 1A (hex). It is read-only and is cleared whenever it is read as well as

when $\overline{RST}$ is asserted. It is an 8 bit counter contained in bits 7 through 0 of the register. Bits 15 through 8 of the register will always be read as zeros. The LE_CTR bit in the INTR_EVENT register is set whenever the counter reaches the value contained in the LE_THRESHOLD register. The counter will continue to count past this point. When the counter overflows (reaches 256) it wraps to zero and continues to count.

The Link Error Event Counter is part of the Link Error Monitor (LEM) and is implemented in the PLC. The LEM monitors Bit Error Rate (BER) of an active link and detects and isolates physical links having an inadequate BER, e.g. due to a marginal link quality, link degradation or connector unplugging.

In addition to the counter, the PLC also contains logic to detect link error events. Link error events are defined in Table 9.

Link Error Event Threshold Register (LE_THRESHOLD)

The Link Error Event Threshold register has address 05 (hex). It is readable and writeable and is cleared on the assertion of $\overline{RST}$. Bits 7 through 0 of this register contain a value that controls when the LE_CTR bit in the INTR_EVENT register is set. Whenever the value in the LINK_ERR_CTR reaches the value contained in this register the LE_CTR bit will be set. Bits 15 through 8 are ignored and will always be read as zeros.

Interrupt Registers

The PLC has two interrupt registers which correspond bit-for-bit. One of the registers contains bits set by interrupt events and the other a mask which enables or disables the assertion of the $\overline{INT}$ pin due to a corresponding interrupt event.

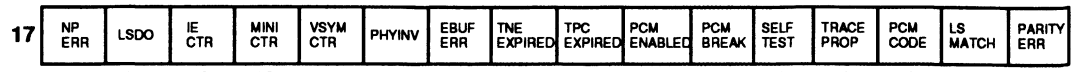
Interrupt Event Register (INTR_EVENT)

The Interrupt Event Register (INTR_EVENT) has address 17 (hex). It is read-only and is cleared whenever it is read as well as when $\overline{RST}$ is asserted. It is used by the PLC to report events to the node processor. Individual bits are set by the PLC for the particular event occurrences. When an interrupt is generated (via the $\overline{INT}$ pin), the node processor should read this register to identify the source(s) of the interrupt.

Note that while the RUN_BIST bit in the PLC_CNTRL_A register is set, all interrupts are masked (prevented from asserting the $\overline{INT}$ pin) except BIST_DONE. Since this is the only interrupt that can occur in this situation, BIST_DONE need not occupy a bit in the INTR_EVENT register. The interrupt is cleared by clearing the RUN_BIST bit in the PLC_CNTRL_A register.

The INTR_EVENT register bit assignments are listed in Table 7.

Addr (Hex) INTR-EVENT



15535-013A

Table 7. INTR_EVENT Register

Bit	Name	Definition
15	NP_ERR	An event indicating that the Node Processor has requested a read or write to an invalid register. This case includes a write to a read-only register (such as this one), a read of a write-only register, a write to a XMIT_VECTOR or VECTOR_LENGTH register when PCM_SIGNALLING is set, a write to the TPC Timer register while the PCM is not in the MAINT state, and a write to the TNE Timer register while the PCM is not in the MAINT state or NOISE_TIMER is set.
14	LSDO	An event indicating that Signal Detect has become asserted, that is, the SDO input pin changed to a 1.
13	LE_CTR	An event indicating that the Link Error Event Counter has reached the value contained in the LE_THRESHOLD register.
12	MINI_CTR	Indicates that either of two events has occurred in the MIN_IDLE_CTR: the Idle Counter Minimum Detector has changed to a lower value; or, the Minimum Idle Gap Counter has incremented or overflowed, depending on the MINI_CTR_INTRS bit in the PLC_CNTRL_A register.
11	VSYM_CTR	An event indicating that a Violation Symbol Counter has incremented or overflowed, depending on the VSYM_CTR_INTRS bit in the PLC_CNTRL_A register.
10	PHYINV	An event indicating that the Physical Layer Invalid signal has been asserted.
09	EBUF_ERR	An event indicating that the Elasticity Buffer has detected an overflow or underflow.
08	TNE_EXPIRED	An event indicating that the TNE Timer has expired, i.e. reached zero.
07	TPC_EXPIRED	An event indicating that the TPC Timer has expired, i.e. reached zero.
06	PCM_ENABLED	An event indicating the PCM has asserted SC_JOIN, has completed scrubbing, and is in the ACTIVE state.
05	PCM_BREAK	An event indicating the PCM has entered the BREAK state.
04	SELF_TEST	An event indicating Quiet or Halt Line State has been received while the PCM is in the TRACE state.
03	TRACE_PROP	An event indicating that Master Line State has been received while the PCM is in the ACTIVE or TRACE state.
02	PCM_CODE	An event indicating the PCM has completed transmitting the last bit in the vector written to the XMIT_VECTOR register and has received the corresponding bit of the RCV_VECTOR, or that the Link Confidence Test has completed. In the case where signalling has completed, PCM_CODE will not be set until the RCF flag has been set again.
01	LS_MATCH	An event indicating that the line state detected equals the line state in the MATCH_LS field of the PLC_CNTRL_B register.
00	PARITY_ERR	An event indicating that a parity error has been detected on the TX 9–0 input pins.

Interrupt Mask Register (INTR_MASK)

The Interrupt Mask Register (INTR_MASK) has address 02 (hex). It is readable and writeable. It allows the disabling of interrupts caused by specific events. The INTR_MASK contains a bit that corresponds to each bit of the INTR_EVENT register that, when clear, prohibits that condition from causing an interrupt to the node processor. For each set bit, the setting of the corresponding bit in the INTR_EVENT will generate an interrupt to the node processor via the $\overline{INT}$ pin of the PLC. Note, however, that the operation of a bit in the INTR_EVENT remains unchanged by the state of the corresponding bit in the INTR_MASK. All bits of this register are cleared with the assertion of $\overline{RST}$.

Addr (Hex) — **INTR-MASK**

02	NP ERR	LSDO	IE CTR	MINI CTR	VSYM CTR	PHYINV	EBUF ERR	TNE EXPIRED	TPC EXPIRED	PCM ENABLED	PCM BREAK	SELF TEST	TRACE PROP	PCM CODE	LS MATCH	PARITY ERR
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

15535-013A

Built In Self Test Register

In addition to a bit in the PLC_CNTRL_A register and a bit in the INTR_EVENT register, Built In Self Test requires one register.

Built In Self Test Signature Register (BIST_SIGNATURE)

The Built In Self Test Signature register (BIST_SIGNATURE) has address 15 (hex). It is a 16 bit, read-only register that contains the resultant signature after execution of the chip's self test. After BIST has been completed (signaled by the $\overline{INT}$ pin being asserted), this register should be read and its contents compared against the known good signature for the PLC to determine whether the chip has passed its self test. The value of the BIST signature is 6ECD (hex).

Framer

The Framer accepts five bit wide parallel data as well as the recovered clock from the Physical Data Receiver (PDR) chip. Generally, data received by the Framer is not framed into proper FDDI symbols. The Framer is used to align the incoming data to form proper symbols before the data is passed onto the Elasticity Buffer. A starting delimiter that is used at the beginning of each frame is detected by the Framer and used to determine proper symbol boundaries for the data. The Framer has been designed such that the starting delimiter (the JK symbol pair) can be detected independent of previous framing.

Elasticity Buffer

The purpose of the Elasticity Buffer is to perform the necessary buffering in order to allow the passing of data between different FDDI stations with independent station clocks. The Elasticity Buffer consists of an 80-bit buffer and some control circuitry. The buffer is used to compensate for the differences in the transmit and receive clock frequencies in the station. Data is clocked into the buffer by the recovered byte clock and clocked out of the buffer by the byte clock. The recovered clock is also used to drive all the input circuitry including the input controller and the local input pointer. The byte clock is used to drive the output circuitry including the output pointer, the output controller, the overflow/underflow detection circuitry and the output buffer. Note that the Elasticity Buffer uses a different version of the byte clock than the rest of the PLC chip. This version is generated on chip from LSCLK.

Smoother Operation

The Smoother resides in the Elasticity Buffer. The main purpose of the Smoother is to add and delete Idle symbols into the data stream when the Smoother detects an inadequate or a surplus number of Idles between frames.

The Smoother function is necessary because the Elasticity Buffer may delete symbols from the preamble of a frame. If multiple PHY Elasticity Buffers delete symbols from the same preamble, then the number of Idle symbols in that preamble can reach a value resulting in a loss of that frame. This may happen because according to the ANSI PHY document,

1) An Elasticity Buffer is not required to recenter on preambles shorter than four symbols,
2) MAC is not required to repeat frames with preambles shorter than two symbols, and
3) MAC is not required to copy frames with preambles shorter than twelve symbols.

The Smoother absorbs surplus symbols from longer preambles and redistributes them into shorter preambles. The smoothing function is capable of inserting additional preamble symbols into repeated preambles shorter than fourteen symbols. The Smoother attempts to maintain 7 Idle bytes (or 14 Idle symbols) between frames. If there are less than 7 Idle bytes the smoother may inject Idle bytes onto the data path. If there are more than 7 Idle bytes in the preamble the Smoother may delete at least one Idle byte of the longer preamble.

Line State Machine (LSM)

In the FDDI network a special group of symbols, called Line State Symbols (Q – Quiet, H – Halt, I – Idle) are transmitted to establish the physical connection between neighboring stations. These Line State Symbols are unique in that they may be recognized independently of symbol boundaries.

The LSM constantly monitors symbol pairs coming from the Elasticity Buffer. The current symbols pair is encoded (ENC_CSP) and compared to the encoded value of the previous symbol pair (ENC_PSP). The symbol pairs are counted by the Symbol Pair Counter (SYM_PR_CTR – bits 2–0 in the PLC_STATUS_A Register) until a Line State is reached. Once a Line State is reached the SYM_PR_CTR is stopped, the new line state (LINE_ST – bits 7–5 in the PLC_STATUS_A Register) is stored and the UNKN_LINE_ST bit is reset to zero. Upon receiving the first symbol pair that is not identical to the previous symbol pair (and is not a JK or noise symbol pair) the SYM_PR_CTR is started and UNKN_LINE_ST is set to 1 until conditions for the next Line State are met.

The recognition of these Line States is reported to the PCM, which uses this information for insertion and removal of the station from the ring, ring recovery and maintenance. A change in the value of LINE_ST is reported to the Node Processor by means of an interrupt which can be enabled or disabled by setting the MATCH_LS bits in the PLC_CNTRL_B register.

The LSM is reset into the NOT_ACTIVE state with LINE_ST = NLS, UNKN_LINE_ST = 0, SYM_PR_CTR = 000 and PREV_LINE_ST = QLS.

The function of the LSM State Machine is described in the following Table 8.

Table 8. LSM State Descriptions

State	Description
LSM0	This is the NOT ACTIVE state. The LSM is in this state whenever LINE_ST equals anything other than ALS. A transition to LSM1 will occur whenever ENC_CSP = JK.
LSM1	This is the ACTIVE state. The LSM will stay in this state only if ENC_CSP = JK, DATA, or II (if ENC_CPS = I I then only if ENC_PSP not = I I). Anything else will cause a transition to LSM0.

Link Error Monitor (LEM)

The Link Error Monitor provides an indication of the inbound link quality to the Physical Connection Management entity. The PCM uses this information to determine if the Link Confidence Test passes to establish a new connection. Once a link is active the PCM continually runs a Link Error Monitor test to detect and isolate links having an inadequate bit error rate.

The LEM hardware consists of a detector, accumulator and threshold element. The detector is a state machine which constantly monitors incoming symbol pairs on the receive path. When Link Error Events are detected they are counted by the 8-bit Link Error Event Counter (LINK_ERR_CTR). When the LINK_ERR_CTR matches the count written to the Link Error Event Threshold Register (LE_THRESHOLD) the LE_CTR bit in the INTR_EVENT register is set.

A Link Error Event is defined in Table 9 below. Note that a number following an H or V symbol indicates the value of that symbol's encoding. For instance, H2 is the symbol "00010", V5 is the symbol "00101", etc.

Table 9. LEM Error Events

Noise Events	Exceptions
Transition from Idle Line State to Noise Line State or Unknown Line State	When the symbol pair which causes the transition is followed by: QQ, QH, HQ, or HH
When in Active Line State, detection of the symbol pair: XV', V"X, J ~K, ~JK, or I D where: V' = H1, H2, H8, H16, V3, V5, V6, V12, or J V" = H1, H2, H8, H16, V3, V5, V6, V12, or K D = n, R, S, or T X = don't care ~K = not K; ~J = not J	None
When in Active Line State, detection of the symbol pair: I I followed by D X I I followed by I D	None
Other transitions from Active Line State to Noise Line State or Unknown Line State	When the symbol pair whichH4 H4, causes the transition is followed by: H4 Q, Q H4, I I, H4 I, or JK

Physical Connection Management (PCM)

Connection Management (CMT) defines the operation of Physical Layer (PHY) insertion and removal, and the connection of PHY entities to the Media Access Control (MAC) entities. Physical Connection Management (PCM) is a subset of CMT. Fundamental to this task is the management of a connection between two physical attachments (PHYs) in adjacent stations. It is the job of the PCM state machines in both stations to cooperate in forming a connection between the two PHYs within the rules established by the Connection Management.

The FDDI SMT ANSI Standard defines the following types of physical attachment:

A: Dual ring PHY entity connected to Primary Ring In, Secondary Ring Out

B: Dual ring PHY entity connected to Secondary Ring In, Primary Ring Out

M: Concentrator PHY entity type "Master" to provide connection within the concentrator tree

S: Single attachment PHY entity type "Slave", intended to be attached to a PHY of type M within a concentrator tree.

Figure 5 illustrates different connection types.

CMT defines the type of physical connection between two physical attachments. PCM consists of two entities; the PCM State Machine and the PCM Pseudo Code. The PLC chip implements the state machine, while the pseudo code is implemented in SMT software. SMT software decides the acceptability of connections and communicates it to the neighboring PHY.

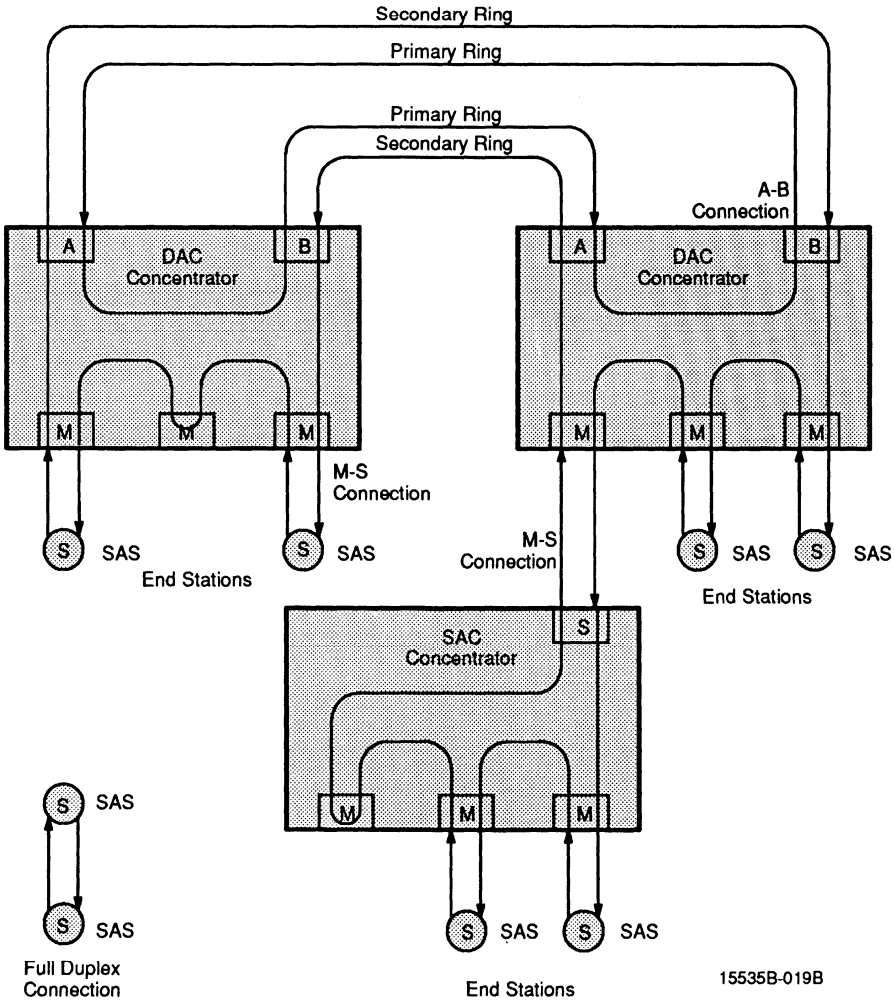


Figure 5. Illustrations of Connection Types

The Physical Connection Insertion (PCI) State Machine works in conjunction with the PCM State Machine. It controls ring scrubbing and the insertion and removal of a station on the ring.

PCM Operation

The PLC implements the PCM state machine as specified in the ANSI FDDI SMT standard. By only allowing a specific set of connection types, CMT secures a deterministic ring topology, independent of the sequence of station power on, etc. The primary purpose for the PCM is to enforce these allowable connections. The local PCM announces its attachment type to the remote PCM and listens for the type of attachment from the remote PCM. If they are compatible, the local PCM accepts the connection, reporting the type of connection to the station configurator. Once the connection type has been established, the two PCMs share in testing the pair of physical links between them. If this is successful, the link can then be configured into the ring. The bit signaling protocol is implemented in a fashion which reduces the software processing overhead considerably while at the same time allow enough flexibility to change the actual pseudo code.

PCM State Machine

The PCM State machine implements the connection sequence for establishing the physical connection into the ring. The state machine is as described in the SMT document. The PCM state machine uses various timers whose expiration values are programmable by the various time registers. The time registers that are relevant to the PCM state machine are the Minimum Connect State (C_Min), Minimum Line State Transmit Time (TL_MIN) Minimum Break (TB_Min), Signalling timeout (T_Out), Link Confidence Test (LC_Length)and Noise time (NS_Max). The current state of PCM is readable through the PLC_Status_B Register.

The PCM State machine is started by PC_Start signal from the node processor as indicated by PCM_CNTRL bits of PLC_CNTRL_B. The PCM State machine can be brought to the OFF state (Stop connection) also by programming PCM_CNTRL bits of PLC_CNTRL_B.

PCM flags that are readable by the Node Processor through the status register of PLC include Line State Flag (LSF), Receive Code Flag (RCF) and Transmit Code Flag (TCF).

Once the connection is established and the ring is scrubbed, PCM indicates the event through the PCM enabled bit of the INTR_EVENT register.

The function of the PCM State Machine is described in Table 10.

Psuedo Code Bit Signaling (PCS)

As a part of the PCM process, before the connection is established, a sequence of bits are communicated through the physical link. These bits as defined in the standard convey the following information:

1) Normal or Escape Sequence (escape sequence is not defined by the standard),
2) The type of Physical connection (Slave, Master, Peer A or Peer B),
3) The acceptance of the connection,
4) The length of the Link Confidence Test (LCT): short, medium, long or extended
5) MAC for LCT,
6) LCT Pass/Fail,
7) MAC Loopback, and
8) MAC output connected to this PHY.

The above information is conveyed in the first 10 bits of the standard pseudo code bit signalling sequence. If more bits are needed, more information up to a maximum of 16 bits can be sent through this process.

The normal operation of the PCM is as follows. When the PCM is in the OFF state all the parameter registers and the configuration registers are loaded with the appropriate values. The VECTOR_LENGTH register is written with the value n-1 (n = the number of bits to be transmitted). Next, the XMIT_VECTOR register is written with the bit pattern which is to be transmitted. PC_Start is then written into the PLC_CNTRL_B register. The PCM then transitions through the BREAK, CONNECT and NEXT states. It then transitions back and forth between the NEXT and the SIGNAL states until all the bits in the XMIT_VECTOR register are transmitted. It causes Master Line State to be sourced to signal a zero bit and Halt Line State to be sourced to signal a one bit. While it transmits all the bits it also receives the corresponding bits from the remote station and forms a Receive Vector which is stored in the RCV_VECTOR register. When all the bits are transmitted the PCM_CODE Interrupt bit is set. The Node Processor can then read the RCV_VECTOR register. (**Note**: The PCM is still in the NEXT state).

If for any reason (other than PC_Start) the PCM state machine transitions to the BREAK state, then a PC_Start has to be issued before the connection process can begin again. This is to allow the VECTOR_LENGTH and the XMIT_VECTOR to be re-initialized. Also, any transition to the BREAK state sets the PCM_BREAK interrupt and writes the reason for the transition in the BREAK_REASON field in the PLC_STATUS_B register.

Typically, three bits are written into the XMIT_VECTOR register in the beginning. After they are received, the received bits are read by the node processor to know the connection type. Then the node processor decides if the connection is acceptable and flags the next bit. On receipt of the corresponding bit from the neighbor, the node processor decides the length of the Link Confidence Test and communicates it through the next two bits. On receipt of the corresponding bits from the neighbor, the node processor communicates if it wants to perform LCT through the MAC. After receipt of corresponding bit from the neighbor, the LCT is performed. If the length of the LCT is longer, then the node processor will set the LONG bit in the PLC_CNTRL_B register. If LONG bit is set, the node processor has to issue a PC_SIGNAL command to progress the sequence and communicate the status of LCT in the next bit.

On receipt of the corresponding bit from the neighbor, the MAC LOOPBACK bit is sent. On receipt of MAC LOOPBACK bit from the neighbor, the MAC LOOPBACK is performed based on the bit information. Once the MAC LOOPBACK is finished, the last bit is communicated indicating if the MAC output is going to be connected to this PHY.

After the LCT is completed (i.e. after LC_LENGTH, or after Halt or Master Line State is received) the PCM_CODE interrupt is set. If the Node Processor decides to transmit more signaling bits it should load the VECTOR_LENGTH with a new value of n and then the XMIT_VECTOR register with the bit pattern to be transmitted. The PCM again starts transmitting these bits and alternates between NEXT and SIGNAL states until all bits are transmitted upon which the PCM_CODE interrupt is set again.

This sequence continues until all the bits are transmitted and the Node Processor writes PC_JOIN in the PLC_CNTRL_B register. The PCM then leaves the NEXT state and enters the JOIN state. Setting these bits has no effect when the PCM is not in the NEXT state or when the PCM_SIGNALING bit is set. However, if this bit is set even though LCT is not finished yet, then LCT will be aborted and the PCM join sequence will be initiated.

Noise Detection Mechanism

The TNE Timer in the PCM times the period between the receptions of the Idle Line State. This timer is loaded with the NS_MAX parameter when Line State Machine leaves the Idle Line State. The TNE Timer keeps counting the Noise until Idle Line State is again detected. While in the ACTIVE state if this timer expires then the PCM will break the link and transition to the BREAK state. In the ACTIVE state the TNE Timer starts counting noise only after LSF is set. If PC_Trace is set and the TNE Timer expires in the same cycle then the transition to the TRACE state is taken. This timer is ignored in all the PCM states except the ACTIVE state.

Noise In MAINT State

If the NOISE_TIMER bit in the PLC_CNTRL_A register is not set then the Node Processor can write the TNE Timer if the PCM is in MAINT state. If the NOISE_TIMER bit is set then the TNE Timer is used in the MAINT state to time the Noise as described above. If the TNE Timer expires then the TNE_EXPIRED bit in the INTR_EVENT register is set.

Operation In TRACE State

In the ACTIVE state if Trace Propagation (i.e., receipt of Master Line State) is detected then the TRACE_PROP interrupt is set. In the ACTIVE state if PC_Trace is received and a transition is made to the TRACE state then the station remains inserted, Master Line State is sourced on the TDAT(4–0) port, and no scrubbing is performed. Again in this state if Master Line State is detected, the TRACE_PROP interrupt is set. If Quiet Line State or Halt Line State is detected then the SELF_TEST interrupt is set.

Table 10. PCM State Description

State	Description
PC0(OFF)	The PCM enters the OFF state whenever the $\overline{RST}$ pin is asserted or whenever the PCM_CNTRL field of the PLC_CNTRL_B register is set to 11 (PC_Stop). The PCM stays in this state until PC_Start is issued or the PC_MAINT bit is set.
PC1(BREAK)	This is the entry point in the start of a PCM connection. The PCM enters this state when PC_Start is issued, or while it is in the process of forming a connection when any of various error conditions occur (such as receipt of Quiet Line State, a timeout, etc.).
PC2(TRACE)	The TRACE state is issued to localize a stuck Beacon condition. It is entered when PC_Trace is issued while the PCM is in the ACTIVE state.
PC3(CONNECT)	This state is used to synchronize the ends of the connection for the signaling sequence. It is entered from the BREAK state.
PC4(NEXT)	This state is used to separate the signaling performed in the SIGNAL state and to perform the Link Confidence Test. It is entered from the CONNECT state or SIGNAL state.
PC5(SIGNAL)	In this state individual bits of information are communicated across the connection by transmitting either Halt symbols or alternating Halt and Quiet symbols (Master Line State). The PCM transmits and receives bits of information at the same time. This state is entered from the NEXT state.
PC6(JOIN)	This state is the first of three states that leads to an active connection. It is entered from the NEXT state.
PC7(VERIFY)	This state is the second state in the path to the ACTIVE state. It will not be reached by a connection that is not synchronized.
PC8(ACTIVE)	The ACTIVE state is the state where the PHY has been incorporated into the ring. It is entered from the VERIFY state.
PC9(MAINT)	This state is used to override the normal PCM operation for test purposes or so that the PCM operation may be done completely in software. In this state the data path configuration and the transmit data stream are controlled by the Node Processor.

PCI Operation

The PCI State Machine works in conjunction with the PCM state machine to control the data paths of the PLC on the MAC side (the RX 9–0 and TX 9–0 paths).

There are three primary functions of the PCI state machine:

1. Provide a bypass path between TX 9–0 and RX 9–0
2. Provide a scrubbing function upon the insertion and removal of a station from the ring.
3. Provide a direct path between the PDT/PDR and the MAC.

The operation of the PCI state machine depends on whether the CLASS_S bit in the PLC_CNTRL_B register is set and whether the PCM state machine is in the MAINT state.

PCI Operation for Non-Class S Type Station

After a reset the PCI state machine will be in the REMOVED state. If the station is not of type Class S, then the PLC will be in the bypass mode where the data input on TX 9–0 is directly output on RX 9–0.

When the PCM state machine enters the ACTIVE state and asserts the SC_JOIN Flag the PCI state machine enters the INSERT_SCRUB state and Idle symbol pairs are sourced on RX 9–0. At the same time, the PCM state machine causes Idle symbols to be output on TDAT 4–0.

The PCI state machine remains in the INSERT_SCRUB state for T_SCRUB length of time, after which it enters the INSERTED state. Upon entering the INSERTED state the PCM_ENABLED interrupt is asserted. In this state a direct path exists from TX 9–0 to TDAT 4–0.

If for some reason the connection is broken and the PCI state machine enters the REMOVE_SCRUB state, Idle symbol pairs are sourced on RX 9–0. Because the PCM state machine is in the BREAK state, Quiet symbols are sourced on TDAT 4–0. While scrubbing is being performed the PCM state machine will not re–start the connection process. The PCI state machine remains in the REMOVE_SCRUB state for T_SCRUB length of time and then enters the REMOVED state.

Note that if the connection is broken while the PCI state machine is in the INSERT_SCRUB state, scrubbing will continue for T_SCRUB length of time and then enter the REMOVED state.

PCI Operation for Class S Type Station

For a Class S type station, the PCI Operation is same as above with one exception. Normally, for a Non-Class S type station, PCI will be in REMOVED state at reset, but for a Class S type station, PCI will be in the INSERTED state. Thus, before entering INSERT_SCRUB or after leaving REMOVE_SCRUB, rather than putting the PLC in the bypass mode, PHY_INVALID is output on RX 9–0.

PCI Operation In MAINT State

When the PCM state machine is in the MAINT state, the PCI state machine does not control the above functions. In this state all the data paths are under the control of software. Software controls the data paths via several control bits in the PLC_CNTRL_A register. Software can also override the PCI functions when the PCM state machine is not in the MAINT state by setting the CONFIG_CNTRL bit in the PLC_CNTRL_B register.

PCI State Machine

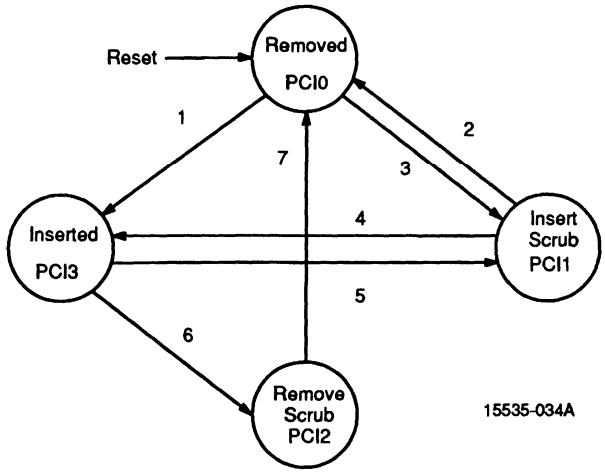
The function of the PCI State Machine is described in Table 11 and Figure 6.

Table 11. PCI State Description

State	Description
PCI0 (REMOVED)	In this state the PCI causes PLC to be bypassed. A transition is made to INSERT_ SCRUB when SET_SC_JOIN signal is asserted. A transition is made to INSERTED if CLASS_S or PCM_MAINT is set
PCI1 (INSERT SCRUB)	In this state scrubbing is performed. A transition is made to INSERTED after T_SCRUB length of time
PCI2 (REMOVE SCRUB)	In this state scrubbing is performed. A transition is made to REMOVED (or to INSERTED if CLASS_S is set) after T_SCRUB length of time
PCI3 (INSERTED)	In this state scrubbing has completed and the data paths exists between the PDT/PDR and the MAC. A transition is made to the REMOVE_ SCRUB state if the START_SCRUBBING signal is asserted. A transition is made to the INSERT_SCRUB state if the SET_SC_JOIN signal is asserted (will only occur if CLASS_S is set).

Note:

User cannot disable PCI.



Notes:

1. Class = S or PCM_MAINT
2. Not (SC_JOIN and not START_SCRUBBING)
3. SET_SC_JOIN
4. TPC > T_SCRUB and (SC_JOIN and not START_SCRUBBING)
5. SET_SC_JOIN
6. Not SET_SC_JOIN and START_SCRUBBING
7. TPC > T_SCRUB

Signals on PCI State Machine:

SC_JOIN:

This signal is output by the PCM state machine and indicates that is has reached the ACTIVE state and scrubbing may be started.

SET_SC_JOIN:

This signal is output by the PCM state machine and is asserted during the clock cycle before SC_JOIN is asserted.

CLASS_S:

This bit in the PLC_CNTRL_B register, when set, indicates that the station is of type CLASS_S.

START_SCRUBBING:

This signal is asserted by the PCM state machine when the station has joined the ring (SC_JOIN is asserted) and a Break condition occurs. It causes the PCI state machine to enter the REMOVE_SCRUB state.

PCM_MAINT:

This signal indicates that the PCM state machine is in the MAINT state.

Figure 6. PCI State Machine

Decoder

The Decoder performs the 4B/5B decoding of received data symbols. The five bits of data from the Elasticity Buffer are decoded into four bits of data and one control bit, with the high order bit being the control bit. The decoded symbol pairs are then sent to the MAC. Although the Decoder operates on symbol pairs, each symbol is decoded independently of the other.

Until the PCM has completed establishing a connection for the physical link, the PHY_INVALID symbol is output by the Decoder. Whether the output of the decoder or the data on TX 9–0 is output on RX 9–0 is dependent on the CLASS_S bit in the PLC_CNTRL_B register. In addition, a Violation symbol (V) shall be generated when an input error condition has been detected, such as an Elasticity Buffer error (buffer overflow or underflow). PHY_INVALID takes precedence over Violation, so if an Elasticity Buffer error occurs while the Current Line State is Quiet, Halt, Master, or Noise then PHY_INVALID (1F in hex) is given to MAC.

The symbol decoding is shown in Table 12.

Table 12. 4B/5B Decoding of Data

Symbol	Encoded Input	Decoded Output
Q	00000	1 0000
I	11111	1 0111
H	00100	1 0100
J	11000	1 1100
K	10001	1 0011
T	01101	1 1101
R	00111	1 0001
S	11001	1 1001
H	00001	1 0100
H	00010	1 0100
V	00011	1 1000
V	00101	1 1000
V	00110	1 1000
H	01000	1 0100
V	01100	1 1000
H	10000	1 0100
0	11110	0 0000
1	01001	0 0001
2	10100	0 0010
3	10101	0 0011
4	01010	0 0100
5	01011	0 0101
6	01110	0 0110
7	01111	0 0111
8	10010	0 1000
9	10011	0 1001
A	10110	0 1010
B	10111	0 1011
C	11010	0 1100
D	11011	0 1101
E	11100	0 1110
F	11101	0 1111

Encoder

The Encoder performs the 4B/5B encoding of data symbols to be transmitted over the physical medium. The four bits of data and one control bit from the MAC are encoded into a unique five bit symbol which is sent to the PDT. Although the Encoder operates on symbol pairs, each symbol is encoded independently of the other.

The symbol encoding is defined in Table 13.

Table 13. 4B/5B Encoding of Data

Symbol	Data Input	Encoded Output
Q	1 0000	00000
I	1 0111	11111
H	1 0100	00100
J	1 1100	11000
K	1 0011	10001
T	1 1101	01101
R	1 0001	00111
S	1 1001	11001
INV	1 1110	11111
INV	1 0010	11111
INV	1 0101	11111
INV	1 0110	11111
INV	1 1111	11111
INV	1 1000	11111
INV	1 1010	11111
INV	1 1011	11111
0	0 0000	11110
1	0 0001	01001
2	0 0010	10100
3	0 0011	10101
4	0 0100	01010
5	0 0101	01011
6	0 0110	01110
7	0 0111	01111
8	0 1000	10010
9	0 1001	10010
A	0 1010	10110
B	0 1011	10111
C	0 1100	11010
D	0 1101	11011
E	0 1110	11100
F	0 1111	11101

Repeat Filter

The main function of the Repeat Filter is to prevent the propagation of code violations and invalid line states from the inbound link to the outbound link. This function is not required if a MAC layer is present in the station configuration (since MAC will not propagate invalid line states and code violations). But certain station configurations consist of only PHY layer entities (such as the path of the secondary ring inside a station with just one MAC in the primary ring). In such cases, a PHY layer implementation is expected to provide the Repeat Filter function.

The Repeat Filter in the PLC filters the symbol stream at the output of the Remote Loopback MUX. Invalid line states are not allowed to propagate through a station; they will be turned into an Idle symbol stream. Also, if the repeat filter detects a corrupted frame, it truncates the frame by transmitting four Halt symbols and then Idle symbols until a JK symbol pair is seen. The Halt symbols will cause the next MAC entity in the logical ring to count the frame as a lost frame.

Another function of the Repeat Filter is called the GOBBLE_BYTE function. When the Repeat Filter detects a fragment, i.e a frame in which Idle symbols appears before the ending delimiter, then it changes the previous symbol pair to Idles. After passing through Repeat Filters in other stations, the fragment will eventually be completely converted to Idles.

The PLC includes the symbol pair wide implementation of the Repeat Filter as defined in the FDDI PHY document.

Data Stream Generator

The Data Stream Generator block uses a multiplexer for the purpose of generating a symbol pair at the request of the PCM via an internal signal bus LS_REQ (or external through control when the PCM is in the MAINT state by using the MAINT_LS bits in the PLC_CNTRL_B register), the Repeat Filter via an internal signal RF-CNTRL (1_0), or transmitting the symbol pair from TX 9–0. The DATA_STRM(9–0) is an internal bus that comes from the Data Stream Generator to the encoder block. The following Table 14 summarizes the operation of this block.

Table 14. Symbol Stream Select Output

LS_REQ(2–0) or MAINT_LS(2–0)	RF_CNTRL (1–0)	DATA_STRM (9–0)
0 0 0	N/A (Note 1)	Quiet Symbol Pair
0 0 1	N/A	Idle Symbol Pair
0 1 0	N/A	Halt Symbol Pair
0 1 1	N/A	Master Symbol Pair
1 0 0	N/A	Quiet Symbol Pair
1 0 1	N/A	Quiet Symbol Pair
1 1 0	0 0	Symbol pair from TX(9–0)
1 1 0	0 1	Idle Symbol Pair
1 1 0	1 0	Halt Symbol Pair
1 1 0	1 1	Idle Symbol Pair
1 1 1	N/A	Quiet Symbol Pair

Note:

1. N/A = Not Applicable

The Data Stream Generator also latches the data each BCLK cycle. This is done for the GOBBLE_BYTE function of the Repeat Filter (see above) which requires that the data be delayed for one clock cycle.

Data Path Muxes

The Receive Data Path and Transmit Data Path of the PLC include six multiplexers (MUXes) for the purpose of altering the normal flow of data through the chip (see chip block diagram). Reasons for altering the data paths are for physical connection insertion and removal and for testing and diagnostics. All receive and transmit data paths internal to the PLC are ten bits (two symbols) wide.

EB Local Loopback Mux

In normal operating mode the EB Local Loopback MUX puts the received input data onto the receive data path of the PLC prior to the Framer.

When the EB_LOC_LOOP bit in the PLC_CNTRL_A register is set or when the built–in self test is running, the MUX sets a loopback path in the PLC chip just at the PLC to PDT/PDR interface. Data from the PLC transmit path are looped back to the input of the Framer. This creates a path whereby data from a MAC device can traverse the entire transmit and receive data paths of the PLC and be returned to the MAC device. The built-in self test uses this loopback along with the Remote Loopback to create a loop which covers all of the transmit data path and receive data path.

LM Local Loopback MUX

In normal operating mode the LM Local Loopback MUX puts the data held in the Receive Data Input latch onto the receive data path of the PLC.

When the LM_LOC_LOOP bit in the PLC_CNTRL_A register is set or when the built–in self test is running, the MUX loops back the data in the Transmit Data Output latch onto the receive data path just after the Elasticity Buffer. This loopback path differs from EB_LOC_LOOP in that the Framer and Elasticity Buffer are bypassed.

Bypass MUX

In normal operating mode the Bypass MUX sends the data output by the Decoder to the Receive Data Output latch.

When the SC_BYPASS bit in the PLC_CNTRL_A register is set while the PCM is in the MAINT state, or when the CONFIG_CNTRL bit is set in the PLC_CNTRL_B register, or when the PCI is in the REMOVED, INSERT_SCRUB, or REMOVE_SCRUB state, the output of the BYPASS MUX is put to the Transmit Data Input Latch onto the receive data path. On reset this BYPASS_MUX will be in effect and will put the Transmit Data Input Latch onto the receive data path.

Remote Loopback MUX

In normal operating mode the Remote Loopback MUX puts the data held in the Transmit Data Input latch onto the transmit data path of the PLC.

When the SC_REM_LOOP bit and the EB_LOC_LOOP bit in the PLC_CNTRL_A register are set (and the LM_LOC_LOOP bit is not set) or when BIST is running, this MUX loops back the data from the Decoder onto the transmit data path and is latched at this point. This creates a path whereby data from the PDR can traverse the entire receive and transmit data paths of the PLC and be transmitted to the PDT. BIST uses this loopback along with the Local Loopback to create a loop which also covers all of the receive data path and the transmit data path.

Scrub MUX

The Scrub MUX selects its input from either constant Idle symbol pairs or the output of the BYPASS_MUX.

When the REQ_SCRUB bit in the PLC_CNTRL_A register is set while the PCM is in the MAINT state, or when CONFIG_CNTRL bits is set in the PLC_CNTRL_B register, the PCI is in the INSERT_SCRUB or REMOVE_SCRUB state, the output of the Scrub MUX is Idle symbols. Otherwise transmit data from the BYPASS_MUX is placed on the Receive Data Output Latch.

This MUX is used when the PLC operates in a Concentrator. When a port in a Concentrator is connecting to an end station, Idle symbols are output on RX 9–0 so as to scrub the ring before the station starts putting data onto the ring. When a port in a Concentrator is not connected to another station, the port is bypassed by routing TX 9–0 back out on RX 9–0.

Test Data MUX

In normal operating mode the Test Data MUX sends the data output by the Encoder to the Transmit Data Output Latch.

When the built-in self test is running the Test Data MUX selects the input from the BIST block. This is how BIST inserts pseudo-random test data into the loop it forms with the transmit and receive data paths. This point was chosen to inject test data because it was desired to avoid sending the test data through the Repeat Filter and the Data Stream Generator. Since both of these logic blocks act as filters, coverage of stuck-at faults in other parts of the chip would be reduced if data from these blocks rather than random test data were used.

Data Input/Output

The PLC contains four ports for receiving and transmitting network data: Receive Data Input, Receive Data Output, Transmit Data Input, and Transmit Data Output. The signal timing for these ports is detailed in the Switching Characteristics and Switching Waveforms chapters of this document.

Receive Data Input

RDAT 4–0 is a five bit (symbol wide) data bus going from the PDR chip to the PLC. RSCLK is also input from the PDR chip and is divided by two to get a recovered byte clock. RDAT 4–0 is latched on each rising and falling edge of the recovered byte clock. Following the rising edge of the recovered byte clock, the five bits (symbol) just latched, plus the five bits (symbol) latched by the previous falling edge recovered byte clock edge, are

used internally in the PLC. All data paths inside the PLC are 10 bits (two symbols) wide.

Receive Data Output

RX is a ten bit (symbol pair wide) data bus going from the PLC to the a MAC device in a Single Attachment Station (SAS). In the case of a Concentrator or a Dual Attachment Station (DAS), RX may also go to another PLC. Data is latched inside the PLC on each rising edge of BCLK and is available to the MAC device shortly after this clock edge.

Transmit Data Input

TX is a ten bit (symbol pair wide) data bus going from the MAC device (or in a Concentrator/DAS, from another PLC) to the PLC. The data is latched by the falling edge of LSCLK that precedes the rising edge of BCLK. Then it is latched again by that rising edge of BCLK. Assuming no skew between LSCLK and BCLK, this effectively adds a one half LSCLK period to the hold time provided on TX. Any amount by which BCLK trails LSCLK will subtract from the hold time provided.

Transmit Data Output

TDAT is a five bit (symbol wide) data bus going from the PLC to the PDT. The ten bit wide internal data bus is latched initially by the PLC by each rising edge of BCLK. Bits nine through five are sent on the rising edge of LSCLK following the rising edge of BCLK. Bits four through zero are then sent on the rising edge of LSCLK following the falling edge of BCLK. Data are available to the PDT shortly after each rising edge of LSCLK.

Built In Self Test (BIST)

The Built In Self Test block contains logic to run the PLC Built In Self Test and also contains control logic for the chip's Counter Segmentation Test Mode and Boundary Scan Test Mode.

BIST Operation

The bulk of the PLC data path and state machine logic is tested by BIST. It remains passive during normal chip operation. Under test mode, BIST tests the chip, and returns a signature which verifies the functioning of the chip's logic with a high degree of certainty. Since BIST sits right on the silicon with the rest of the chip, it has the advantage of the optimum observability location: inside the chip.

BIST tests the PLC by circulating pseudo random data throughout the chip. The various subcircuits within the chip are observed as they respond to these data, and a signature based upon their behavior is generated. This signature may be checked against the known correct signature, to verify the functioning of the chip. A single fault in the chip, as long as it is covered by BIST, will cause a different signature to be generated.

The majority of the logic blocks of the PLC sit directly on the chip's data path. These blocks are easily tested by placing pseudo random vectors, generated by the Linear Feedback Shift Register (LSFR), on the data paths, and observing the behavior of the blocks with the Signature Generator.

With this method, data from LFSR are input by the Transmit Data Output latch lines via the Test Data Mux (see Block Diagram on page 2). The test data are looped back onto the receive data path via the EB Local Loopback MUX. The test data traverse the entire receive data path and are fed back to the Signature Generator. The test data are input to the transmit data path via the Remote Loopback MUX. The test data are fed back to the Signature Generator before the transmit data path because the Repeat Filter, Data Stream Generator, and Encoder act as filters which would reduce the fault coverage provided by the test data. Fault coverage is obtained for the Repeat Filter, Data Stream Generator, and Encoder by separate signals fed to the Signature Generator.

The state machines, while somewhat attached to the data path, are more control oriented, and are not likely to respond well to random vectors on the data paths. The LEM, LSM, PCM, PCI, and RF state machines are tested using scan logic. Under test mode, the state registers of the state machines, and their control bits in the registers of the NPI are linked together to form a scan chain. The output of the scan chain drives a bit in the Signature Generator.

BIST is activated with the assertion of the RUN-BIST bit in the PLC_CNTRL_A register. Upon activation, the data path, LFSR, and Signature Generator are initialized, and the latches in the scan chain are placed in scan mode. After initialization, the LFSR and Signature Generator are enabled, and the test proceeds.

When BIST has completed, the signature is frozen, and may be read through the Node Processor Interface. End of test occurs when a value of zero is reached in the LFSR. Using a 16 bit LFSR clocked by the 80 nanosecond BCLK it will take approximately 5.24 milliseconds to circulate 65535 test patterns through the chip. An interrupt to the node processor after RUN_BIST has been asserted signifies the completion of the PLC self test. This interrupt is cleared by clearing the RUN_BIST bit in the PLC_CNTRL_A register (NOT by reading the INTR_EVENT register). BIST is aborted if the RUN_BIST bit is cleared by writing a zero in the RUN_BIST bit in the PLC_CNTRL_A register before BIST completes.

Counter Segmentation Test Mode

The counters (including all timers) in the PLC are designed in such a way, that under Counter Segmentation Test Mode, they break apart into several 4 bit counters. For example, in Counter Segmentation Test Mode, a 16 bit counter becomes four 4 bit counters. These 4 bit counters in parallel, allowing the counters to be tested in $2^4 = 16$ cycles, as opposed to $2^{16} = 65536$ cycles for a 16 bit counter.

Since counter test requires the ability to control the BCLK, this test is not intended for any board level tests or diagnostics. This is a factory test only.

Boundary Scan Test Mode

In Boundary Scan Test Mode, most of the chip input and output latches are linked together to form a scan chain. While this complements BIST, which does not test these latches, the main purpose of this test mode is for board testing. In this mode the I/O latches of the various chips on the board are linked into a large scan chain. By serially shifting data into the scan chain (Boundary Scan Serial Test Mode), then clocking the data in parallel (Normal or Boundary Scan Parallel Test Mode) and then serially shifting the data out, the I/O latches and interconnections between the various chips can be tested.

The order of pins in the scan chain is shown in Table 15. The pin ETEST 0 is the scan chain input and the pin ESCANO is the scan chain output. The pins $\overline{RST}$, LSCLK, BCLK, NPCLK, RSCLK, RESRCK, EBFERR, $\overline{LPBCK}$, SDO, LSR 2–0, ULSB, ENCOFF, ETEST 2–0, PTSTO, NPADDR 4–0, $\overline{INT}$, $\overline{CS}$, and NPRW are not included in the scan chain. Note that only the output portion of the NP 15–0 bus is in the scan chain.

Table 15. Boundary Scan Chain Order

Pin	Type
RDAT0	Input
to	
RDAT4	Input
FOTOFF	Output
TDAT4	Output
to	
TDAT0	Output
TX0	Input
to	
TX9	Input
RXPAR	Input
RXPAR	Output
RX9	Output
to	
RX0	Output
NP 15	Output
to	
NP 0	Output

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65 to +150°C
Ambient Temperature	0 to 70°C
Supply Voltage Referenced to Vss	−0.3 to +6 V
DC Voltage applied to any Pin Referenced to Vss	−0.5 to V_{DD} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Temperature (T_A)	0 to +70°C
Supply Voltage, V_{DD}	+5 V ± 5%

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input Low Voltage		−0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{DD} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA	2.4		V
I_{OZ}	Output Leakage Current (Note 1)	0.4 V < V_{OUT} < V_{DD}	−10	10	µA
I_{IX}	Input Leakage Current (Note 2)	0 V < V_{IN} < V_{DD}	−10	10	µA

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{DD}	Power Supply Current (Note 3)	V_{CC} = Max. f(BCLK, NPCLK) = 12.5 MHz f(LSCLK, RSCLK) = 25 MHz	80	100	125	mA

Notes:

1. I_{OZ} applies to all three-state output pins and bidirectional pins.
2. I_{IX} applies to all input-only pins.
3. V_{IL} = 0.0 V and V_{IH} = 3.0 V for I_{DD} test.

CAPACITANCE (See Note 4)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
C_{IN}	Input pins			10	pF
$C_{I/O}$	Bidirectional pins (Note 5)			10	pF

Notes:

4. Pin capacitance is characterized at a frequency of 1 MHz, but is not 100% tested.
5. Bidirectional and output pins are designed to drive a 50 pF capacitive load.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges

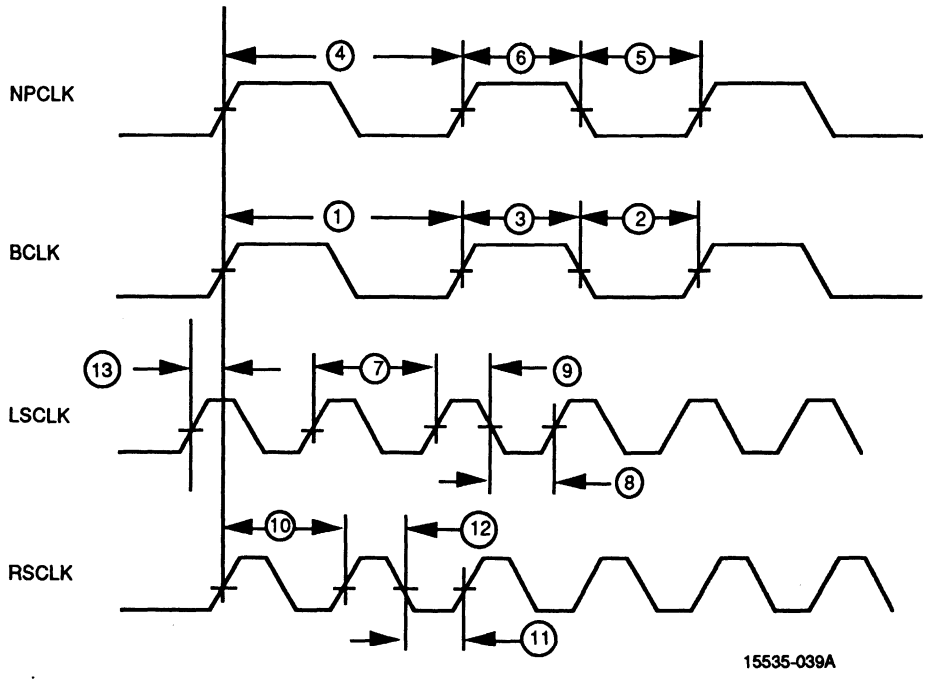
Parameter Symbol	Parameter Description	Min.	Max.	Unit
1	BCLK Period	80		ns
2	BCLK Pulse Width Low	38	42	ns
3	BCLK Pulse Width High	38	42	ns
4	NPCLK Period	80		ns
5	NPCLK Pulse Width Low	38	42	ns
6	NPCLK Pulse Width High	38	42	ns
7	LSCLK Period	40		ns
8	LSCLK Pulse Width Low	15		ns
9	LSCLK Pulse Width High	15		ns
10	RSCLK Period	40		ns
11	RSCLK Pulse Width Low	15		ns
12	RSCLK Pulse Width High	10		ns
13	LSCLK to BCLK Skew	2	8	ns
14	$\overline{CS}$ Setup Time	10		ns
15	$\overline{CS}$ Hold Time	10		ns
16	NPRW Setup Time	5		ns
17	NPRW Hold Time	20		ns
16	NPADDR Setup Time	5		ns
17	NPADDR Hold Time	20		ns
18	NP Driven to High Impedence		30	ns
19	NP Driven	2		ns
20	NP Valid		30	ns
21	NP Invalid	2		ns
22	NP Setup Time	30		ns
23	NP Hold Time	20		
24	$\overline{INT}$ Asserted		40	ns
25	$\overline{INT}$ Deasserted		40	ns
26	RX, RXPAR Valid		25	ns
27	RX, RXPAR Invalid	3		ns
28	TX, TXPAR Setup Time	5		ns
29	TX, TXPAR Hold Time	10		ns
30	RDAT Setup Time	5		ns
31	RDAT Hold Time	8		ns
32	$\overline{LPBCK}$ Valid		25	ns
33	$\overline{LPBCK}$ Invalid	2		ns
34	SDO Setup Time	5		ns
35	SDO Hold Time	15		ns
36	TDAT Valid		25	ns
37	TDAT Invalid	3		ns
32	$\overline{FOTOFF}$ Valid		25	ns
33	$\overline{FOTOFF}$ Invalid	2		ns
38	PTSTO Setup Time	15		ns
39	PTSTO Hold Time	15		ns
32	SCANO Valid		25	ns
33	SCANO Invald	2		ns
40	ENCOFF Setup Time	10		ns
41	ENCOFF Hold Time	10		ns
32	LSR, ULSB, EBFERR Valid		25	ns
33	LSR, ULSB, EBFERR Invalid	2		ns
42	$\overline{RST}$ Pulse Width	20* (BLCK Period)		ns

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

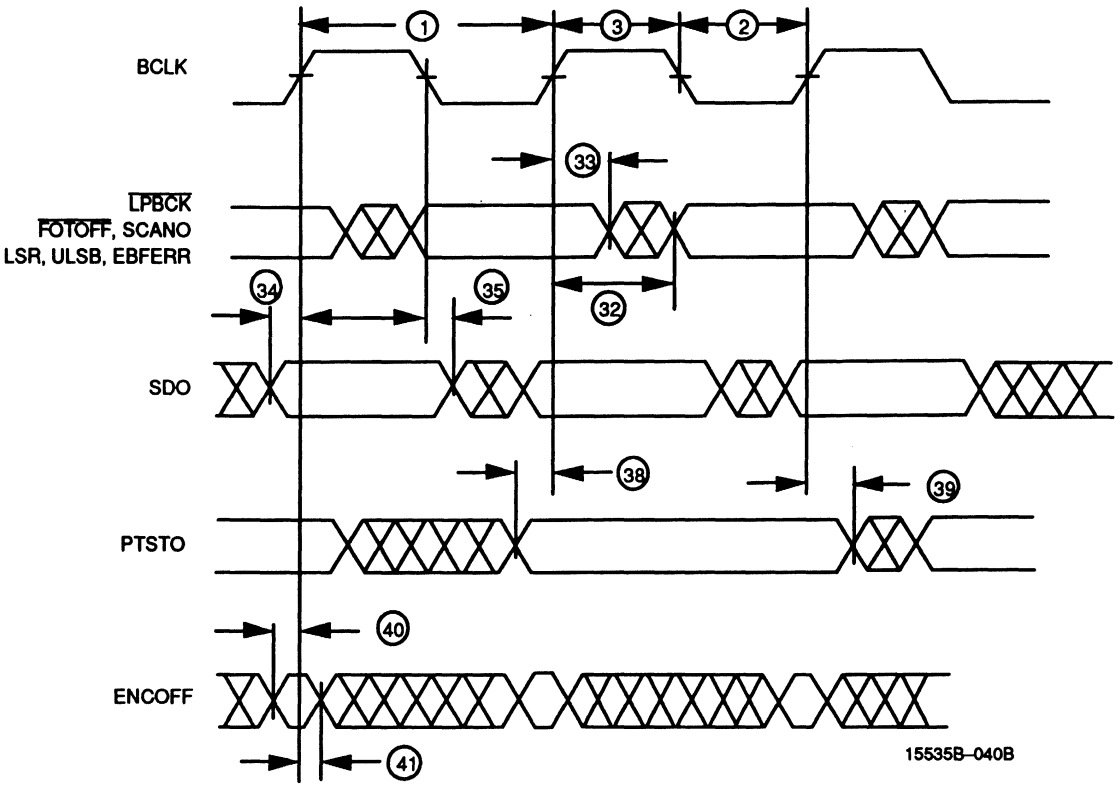
KS000010

SWITCHING WAVEFORMS



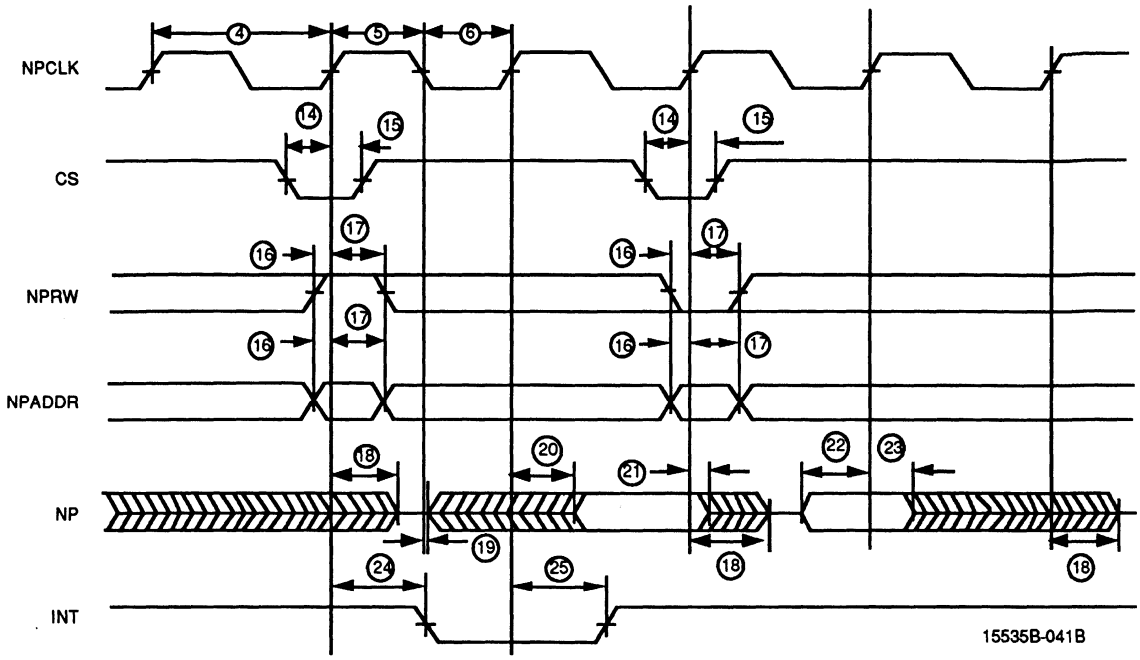
PLC Clock Timing Parameters

SWITCHING WAVEFORMS

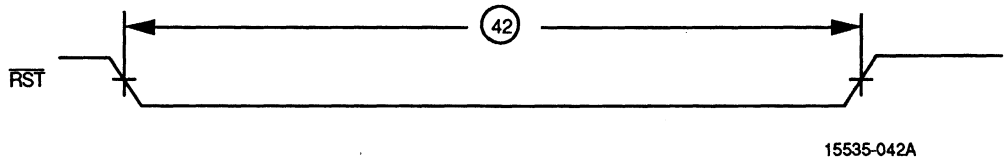


PLC Misc Signals Timing Diagram

SWITCHING WAVEFORMS

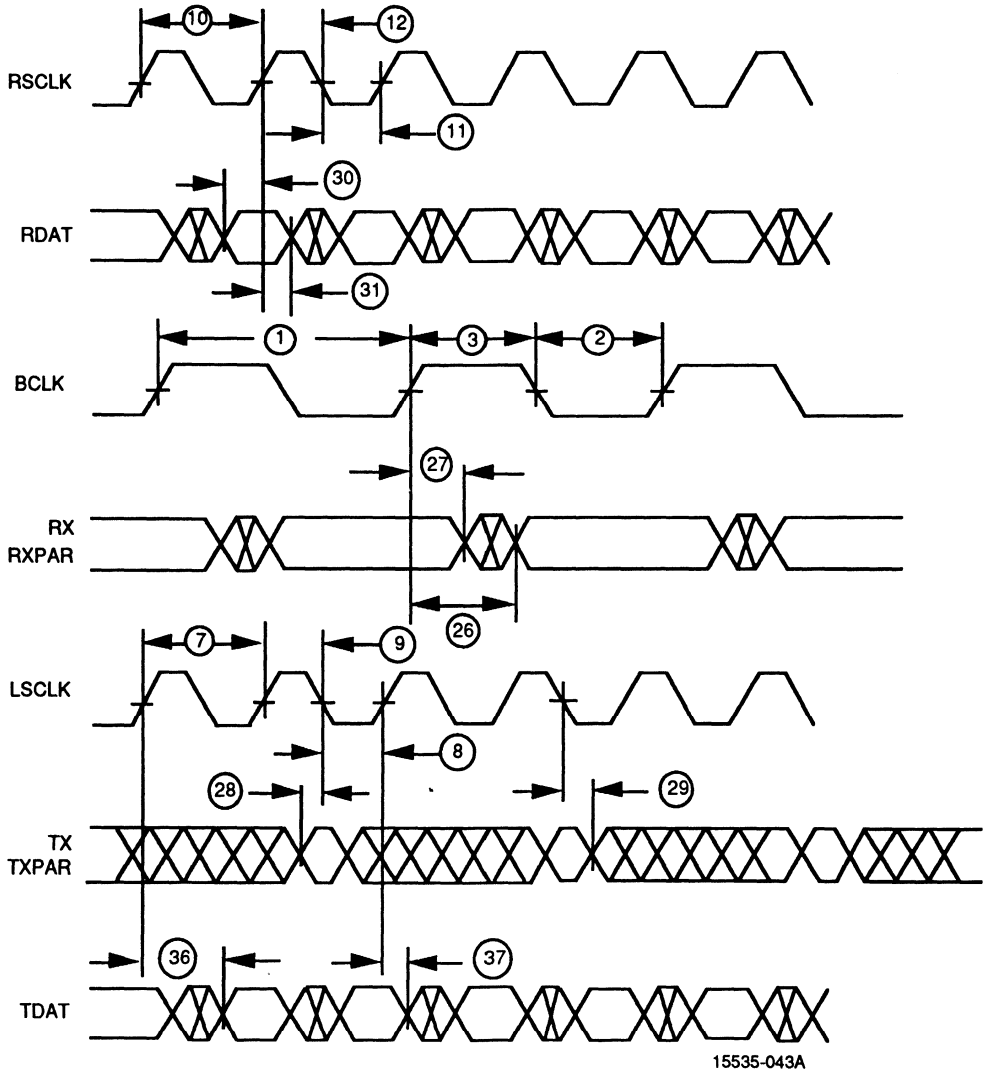


Node Processor Interface Timing Diagram



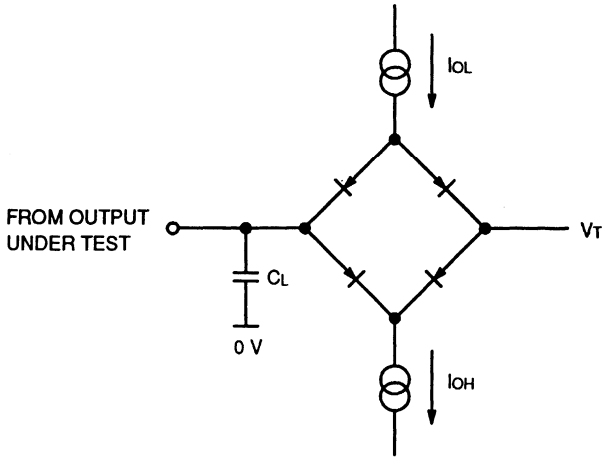
PLC Reset Timing Parameters

SWITCHING WAVEFORMS



PLC Data Interface Timing Diagram

SWITCHING TEST CIRCUIT

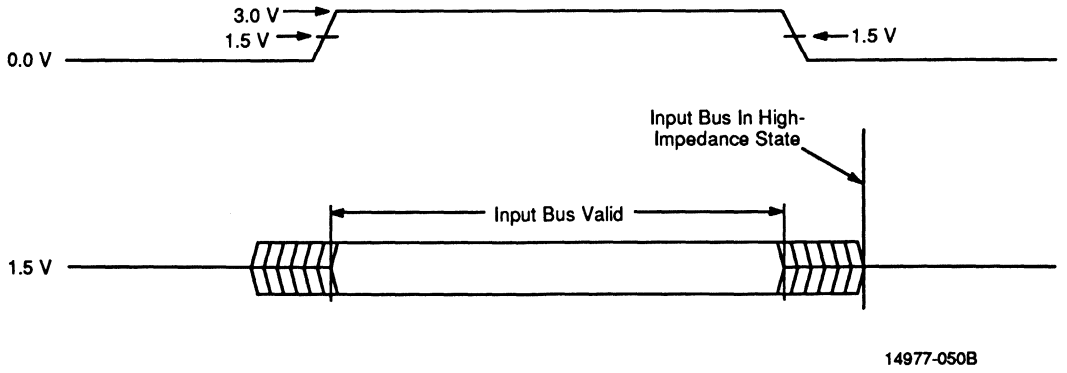


Note:

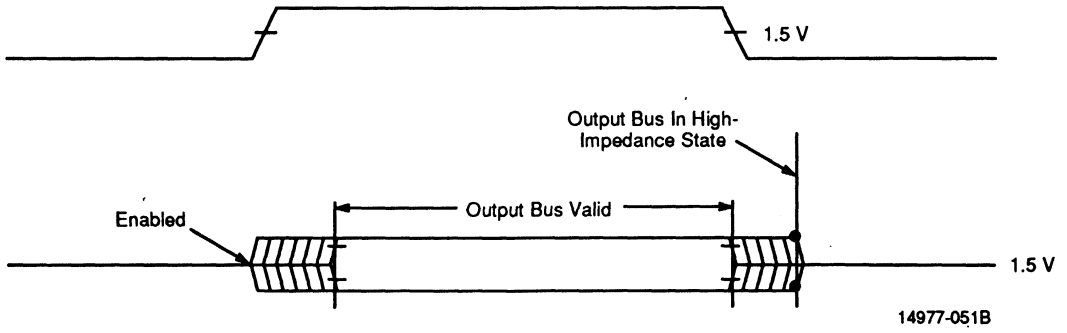
C_L = 50 pF for all bidirectional or output pins.

Standard Test Load

SWITCHING TEST WAVEFORMS



Input Waveform Test Points



Output Waveform Test Points

Preliminary

Am79865/Am79866

Physical Data Transmitter/Physical Data Receiver

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Parallel input to the PDT is a 5-bit encoded NRZ symbol clocked by LSCLK**
- **Parallel output from the PDR is a 5-bit unframed NRZ symbol clocked by RSCLK**
- **The on-chip Phase-Locked-Loop (PLL) only requires an external frequency reference**
- **125 MBaud (100 Mbps) serial link data rate**
- **PECL serial I/Os connect to most Fiber Optic Transmitters and Receivers directly with proper termination**
- **Dedicated pins provide electrical loopback data path**
- **20-pin Plastic Leaded Chip Carrier (PLCC)**
- **Single +5 V power supply operation**

GENERAL DESCRIPTION

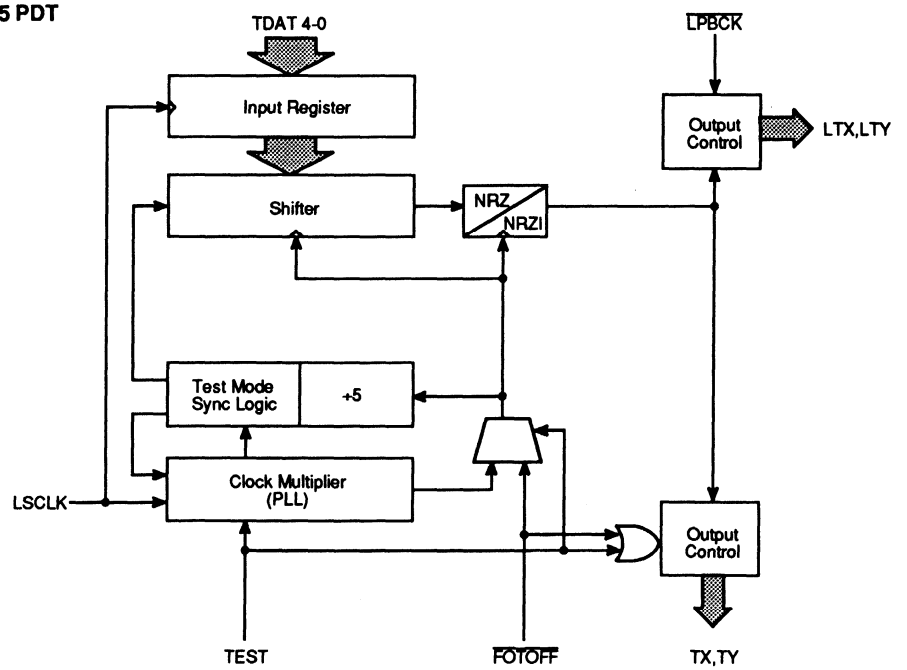
The SUPERNET® 2 FDDI Physical Layer Protocol (PHY) chip set includes the Physical Layer Controller (PLC), the Physical Data Transmitter (PDT) and the Physical Data Receiver (PDR). The PLC, PDT and PDR are collectively known as the AmPHY. The PLC performs FDDI physical layer functions which includes, among others, the 4B5B encoding and decoding.

The PDT converts encoded symbols into a serial NRZI data stream. The on-chip PLL generates a bit rate clock from the LSCLK reference.

The PDR uses a built-in clock recovery PLL to extract clock information from the received data stream. The recovered clock is used for serial-to-parallel data conversion.

BLOCK DIAGRAM

Am79865 PDT

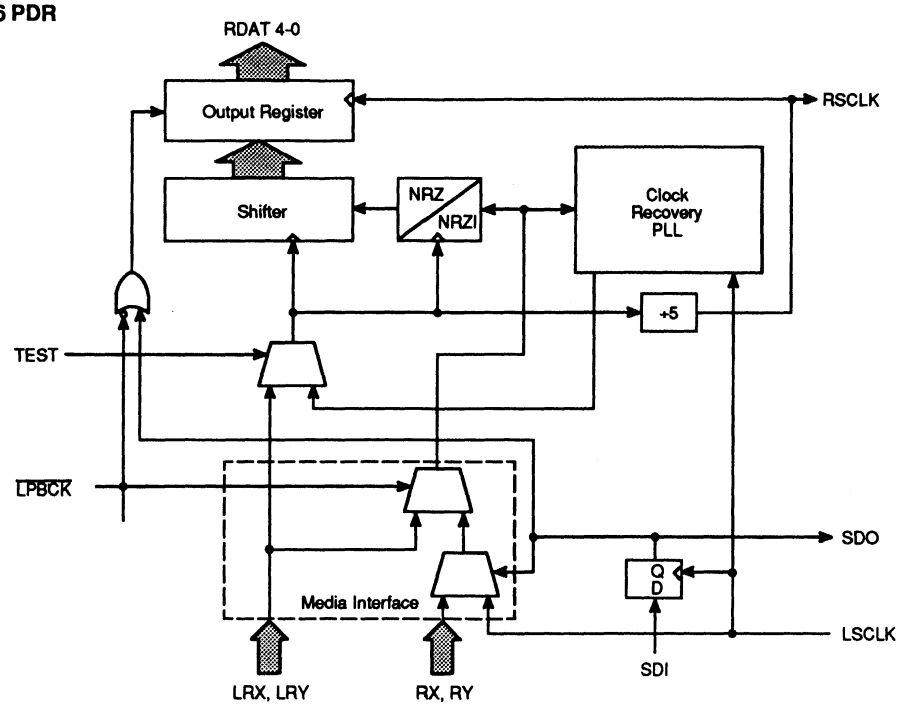


15451-001A

Publication# 15451 Rev. B Amendment/0
Issue Date: October 1991

BLOCK DIAGRAM

Am79866 PDR

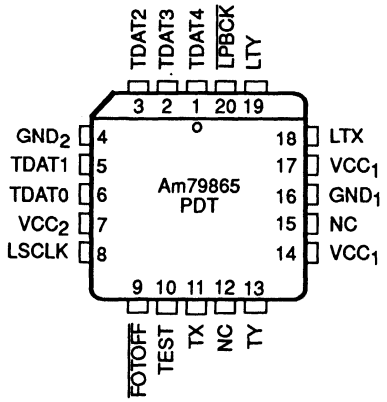


15451-002A

CONNECTION DIAGRAMS

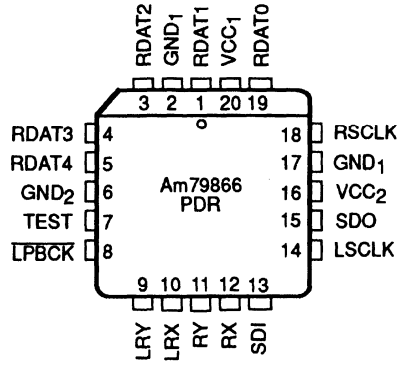
Top View

20-Pin PLCC



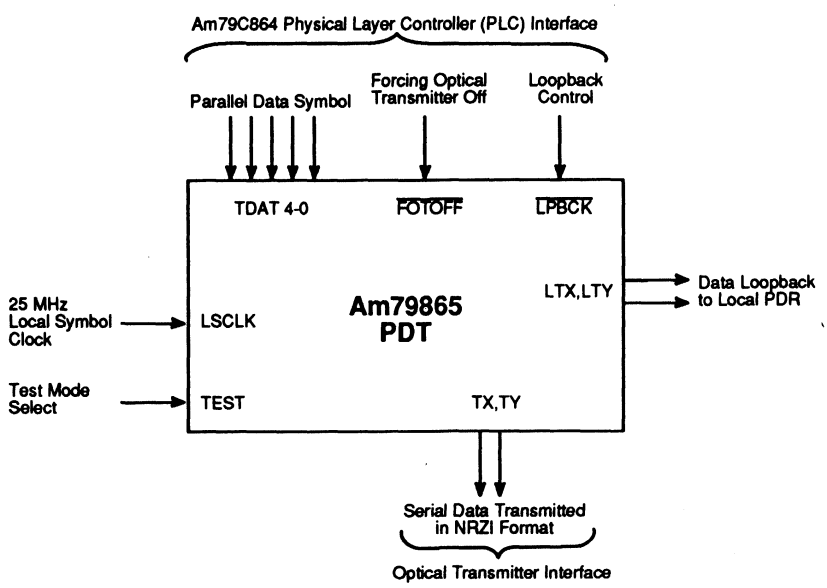
15451-003A

20-Pin PLCC



15451-004A

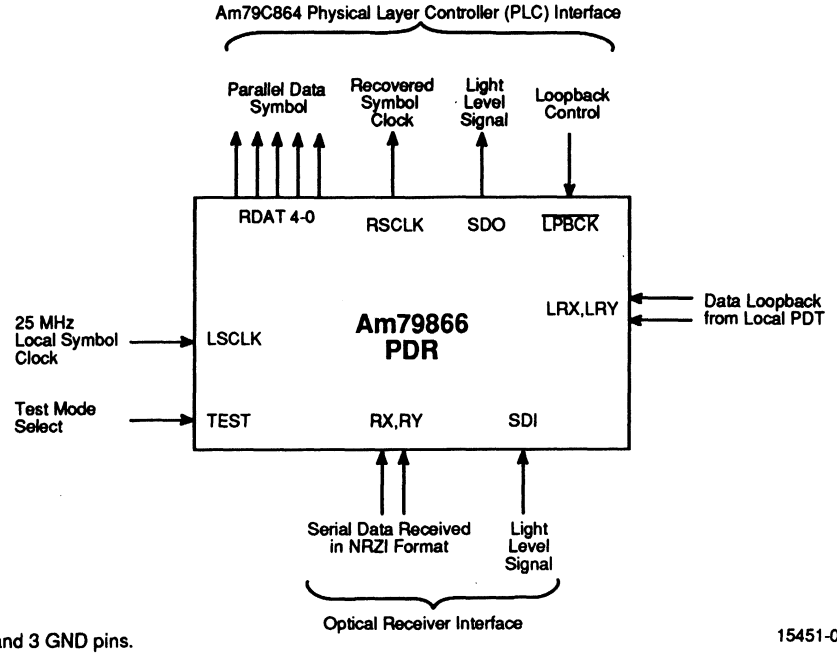
LOGIC SYMBOLS



15451-005A

Note:

1. 3 Vcc pins and 2 GND pins.



15451-006A

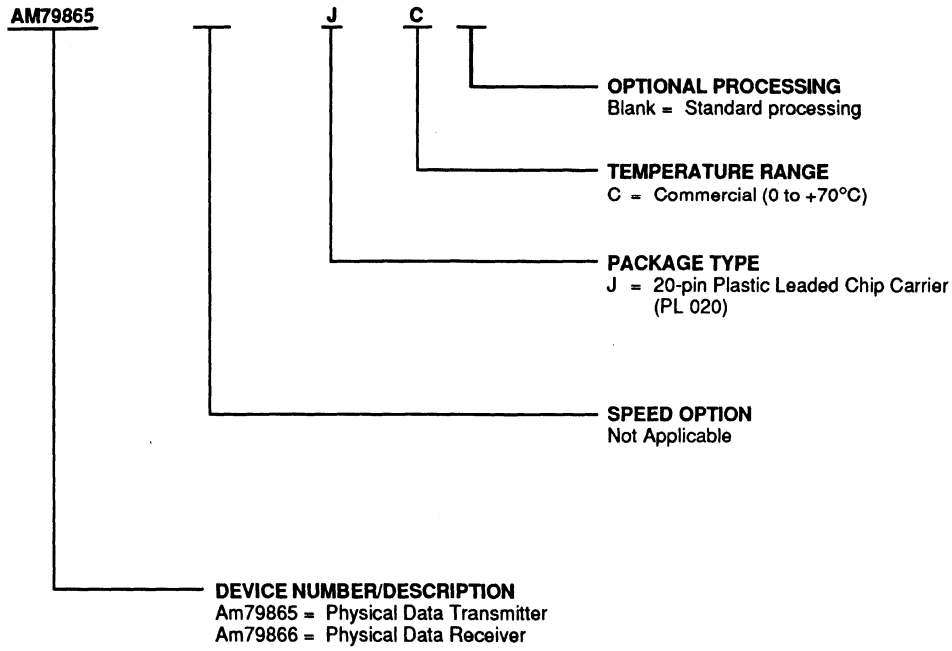
Note:

1. 2 Vcc pins and 3 GND pins.

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

Device Number
Speed Option (if applicable)
Package Type
Temperature Range
Optional Processing



Valid Combinations	
AM79865	JC
AM79866	JC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released valid combinations.

Am79865 PDT PIN DESCRIPTION

TDAT 4-0
Transmit Data (TTL Inputs)

These five inputs accept data symbols from the Am79C864 PLC, latched by the rising edge of LSCLK.

LSCLK
Local Symbol Clock (TTL Input)

This pin supplies the frequency and phase reference to the internal PLL clock multiplier. It should be driven by an external 25 MHz crystal-controlled clock source.

$\overline{\text{FOTOFF}}$
Fiber Optic Transmitter Off (TTL Input, active LOW)

When held LOW, the TX output is forced LOW and TY output is forced HIGH so that the Fiber Optic Transmitter will output logical 0. In test mode, $\overline{\text{FOTOFF}}$ is used as the test clock input and does not control TX/TY.

$\overline{\text{LPBCK}}$
Loopback Control (TTL Input, active LOW)

When asserted, the LTX/LTY outputs transmit the NRZI serial bit stream to the PDR to establish the loopback data path. When deasserted, the LTX output is forced LOW and LTY output is forced HIGH.

TEST
Test Mode Enable (TTL Input)

When asserted, the PDT is in Test mode. For normal operation, TEST pin must be tied LOW.

TX,TY**
Transmit Data (PECL Differential Outputs)

These transmit outputs carry differential NRZI data. They can be forced to logical 0 (TX LOW, TY HIGH) by asserting the $\overline{\text{FOTOFF}}$ input.

LTX,LTY**
Loopback Transmit Data (PECL Differential Outputs)

These differential outputs carry the same signal as TX/TY when the $\overline{\text{LPBCK}}$ input is asserted (LOW). LTX/LTY should be connected to the LRX/LRY pins of Am79866 PDR to perform loopback function. When $\overline{\text{LPBCK}}$ is deasserted (HIGH), LTX is forced LOW and LTY is forced HIGH.

V_{CC1},V_{CC2}
Power Supply

V_{CC1},V_{CC2} are +5.0V nominal power supply pins. V_{CC1} powers all TTL and ECL I/O circuits. V_{CC2} powers all internal logic gates and analog circuits. They must be connected to a common external supply.

GND_1,GND_2
Ground Pins

GND_1 is TTL and ECL I/O ground. GND_2 is the internal logic and analog ground. They must be connected to a common external ground reference.

**All differential PECL outputs carry data at ECL voltage levels referenced to +5.0 V (PECL levels). The external terminations required are shown in the Interface Connection Diagram in the Appendix.

Am79866 PDR PIN DESCRIPTION

LSCLK
Local Symbol Clock (TTL Input)

LSCLK is driven by an external frequency source at the 25 MHz symbol rate. This signal is used as a frequency reference for the PDR clock-recovery PLL.

$\overline{\text{LPBCK}}$
Loopback (TTL Input, active LOW)

When active, $\overline{\text{LPBCK}}$ selects the serial data stream at LRX/LRY inputs as the received data. When HIGH, RX/RY are selected. This function is used during system loopback test to bypass the transmission medium.

TEST
TEST Mode Enable (TTL Input)

When asserted, the PDR is in Test mode. For normal operation, TEST pin must be tied LOW.

RDAT 4-0
Received Data (TTL Outputs)

These 5-bit parallel outputs are clocked by the falling edge of RSCLK and carry the NRZ data symbols to the PLC.

RSCLK
Recovered Symbol Clock (TTL Output)

RSCLK is derived from the clock synchronization PLL circuit. It is synchronous to the received serial data, and is the recovered bit clock divided-by-five. This is a 25 MHz clock.

SDI
Signal Detect Input (PECL Single-ended Input)

SDI typically comes from the fiber optic receiver to indicate that the received optical signal is above the detection threshold. When asserted (HIGH), the data on RX/RY are used for the input to the PDR. When deasserted (LOW), the RX/RY data stream is gated off and the PLL locks onto the LSCLK.

SDO
Signal Detect Output (TTL Output)

SDO is the SDI input synchronized by LSCLK. It has the same logical sense as SDI, i.e., HIGH indicates the received optical signal is above the detection threshold.

RX,RY*
Received Data (PECL Differential Line Receiver Inputs)

These pins receive NRZI data.

LRX,LRY*
Loopback Received Data (PECL Differential Line Receiver Inputs)

This input pair should be connected to the PDT LTX/LTY outputs through properly terminated lines to establish the loopback data path. When $\overline{\text{LPBCK}}$ is asserted, LRX/LRY carry the data to be used as the input to the PDR. In Test mode, LRX/LRY become the test clock input.

V_{CC1},V_{CC2}
Power Supply

V_{CC1},V_{CC2} are +5.0 V nominal power supply pins. V_{CC1} powers all TTL and ECL I/O circuits. V_{CC2} powers all internal logic gates and analog circuits. They must be connected to a common external supply.

GND_1,GND_2
Ground Pins

GND_1 is TTL and ECL I/O ground. GND_2 is the internal logic and analog ground. They must be connected to a common external ground reference.

*RX/RY and LRX/LRY are differential line receivers which have high input sensitivity and wide common-mode range. They can also accept PECL voltage swings and shall be driven by properly terminated transmission lines.

FUNCTIONAL DESCRIPTION

Normal Operation Mode

The Am79865 PDT accepts encoded data symbols at TDAT 4-0 pins. The 5-bit symbol is latched into the PDT by the rising edge of LSCLK, serialized, converted to NRZI format and shifted to the outputs (TDAT4 bit is transmitted first). There are two pairs of serial data outputs capable of driving either Fiber Optic Interface hardware or wire transmission lines without external buffering. The TX/TY pair is connected to the serial link and the LTX/LTY pair is used in the loopback connection to the Am79866 PDR.

The PDT uses LSCLK as the frequency reference to generate the serial link data rate. The external clock source must be crystal controlled and continuous. All of the internal logic of PDT runs on an internal clock that is PLL-multiplied from the external reference source. The PDT's internal PLL is referenced to the rising edges of LSCLK only.

The input clock frequency required to achieve 125 MBaud on the serial link is 25 MHz at LSCLK. In order to generate the serial output waveforms conforming to the FDDI specification, the external reference clock (LSCLK) must meet FDDI frequency and stability requirements. The PDT serial output typically contains less than 0.4 ns peak-to-peak jitter at 125 MBaud. The latency from the LSCLK to the serial output is typically 4 to 6 bits (8 ns/bit).

The Am79866 PDR accepts encoded NRZI serial data on the RX/RY inputs and converts them to NRZ format. It then latches the unframed symbol (5 bits) to the RDAT 4-0 outputs on the falling edge of RSCLK.

The heart of the Am79866 PDR chip is its clock-recovery PLL which extracts encoded clock information from the serial NRZI data stream and recovers the data. The PLL examines every data transition in the received serial stream and aligns its internal bit clock with these data transitions. In order to guarantee the correct operation of the PLL, the encoding scheme (such as the FDDI 4B5B code) must insure adequate transition density of the encoded data stream.

The PDR has input jitter tolerance characteristics that meet or exceed the recommendations of Physical Layer Medium Dependent (PMD) FDDI document. Typically, at 125 MBaud (8 ns/bit), the peak-to-peak Duty-Cycle Distortion (DCD) tolerance is 1.4 ns, the peak-to-peak Data-Dependent Jitter (DDJ) tolerance is 2.2 ns, and the peak-to-peak Random Jitter (RJ) tolerance is 2.27 ns. The total combined peak-to-peak jitter tolerance is typically 5 ns with bit error rate (BER) less than 2.5×10^{-10}.

The PDR's PLL typically has an acquisition time of 100 µs or less when 'Master' symbols (one data transition within ten bits) are received. The acquisition time reduces with increasing transition density in the data stream.

The SDI input qualifies the data at RX/RY. When SDI is LOW, the PDR uses LSCLK as the PLL input and forces LOW at the Output Register. The $\overline{\text{LPBCK}}$ input selects the data source between RX/RY and LRX/LRY. When $\overline{\text{LPBCK}}$ is LOW, the SDI input is ignored.

When SDI is HIGH and the RX/RY input stream contains no data transition for PLL input, the PLL operating frequency range is limited by the LSCLK reference. The observed RSCLK output frequency is generally within 0.5 % of the LSCLK frequency.

Under normal conditions, the frequency of LSCLK multiplied by five must be within 0.25 % of the expected received data for the PLL to operate correctly. (Note, FDDI specifies the two frequencies to be within 50 ppm or 0.005 % of each other.)

Am79865 PDT Functional Block Description

Clock Multiplier

LSCLK supplies the reference frequency which is multiplied by five using an on-chip PLL. The transmission rate and all serialization logic are controlled by the internally generated bit clock.

Input Register

TDAT 4-0 are clocked into the Input Register by the rising edge of LSCLK.

Shifter

Parallel data are loaded from the Input Register into the Shifter at the internally generated symbol boundary, and serially shifted at the bit clock rate.

NRZ-to-NRZI Converter

The NRZ output of the Shifter is converted into NRZI data patterns for transmission.

Output Control

The differential outputs carry the encoded serial NRZI bit stream. The TX/TY pair can be forced to logical 0 (TX LOW, TY HIGH) by asserting $\overline{\text{FOTOFF}}$ input. The LTX/LTY pair can be forced to logical 0 (LTX LOW, LTY HIGH) by deasserting the $\overline{\text{LPBCK}}$ input.

Am79866 PDR Functional Block Description

Clock-Recovery PLL

The clock-recovery PLL separates the input data stream into clock and data patterns. The PLL operating frequency is established by the reference at LSCLK. The PLL is capable of tracking data correctly within ± 0.25 %

of LSCLK (exceeds the frequency range defined by the FDDI specification).

Media Interface

The RX/RY inputs are typically driven by differential PECL voltages, referenced to +5 V. These inputs accept the encoded NRZI serial data. LRX/LRY are also differential line receiver inputs which accept the loopback data stream from the local PDT LTX/LTY outputs.

NRZI-TO-NRZ Converter

Serial data are retimed and associated jitter is removed. Retimed data are converted into NRZ format prior to the Shifter input.

Shifter

The Shifter is serially loaded from the NRZI_TO_NRZ converter, using the recovered bit clock.

Output Register

The Output Register is clocked by RSCLK falling edges. RSCLK is the recovered bit clock divided-by-five and is synchronous to the received serial data.

Test Mode

Asserting PDT TEST input pin forces PDT into its test mode. This allows testing of the internal logic without the PLL clock multiplier. The internal clock source is replaced by the test clock provided at the $\overline{\text{FOTOFF}}$ input. An automatic test system can clock the PDT through functional test patterns at any rate, typically less than 25 MHz, or any sequence to facilitate logic verification.

In PDT test mode, LSCLK strobes data into the Input Register and provides initialization to the internal counter.

The PDR test mode allows testing of the internal logic without the PLL. When TEST is HIGH, the internal clock source is replaced by the test clock provided at the LRX/LRY inputs. (Note: The loopback data path in the Am79866 PDR cannot be tested in test mode.)

An automatic test system can clock the PDR through functional test patterns at any rate, typically less than 25 MHz, or any sequence to facilitate logic verification.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature under bias	–55°C to +125°C
Supply Voltage (V_{CC}) to Ground Potential Continuous	–0.5 V to +7.0 V
DC Voltage Applied to Outputs	–0.5 to V_{CC} Max.
DC Input Voltage	–0.5 V to +5.5 V
DC Output Current	±100 mA
DC Input Current	–30 to +5.0 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)	0°C to 70°C
Supply Voltage (V_{CC})	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Am79865 PDT

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ. (Note 2)	Max.
TTL Inputs: TDAT 4-0, LSCLK, $\overline{\text{FOTOFF}}$, $\overline{\text{LPBCK}}$, TEST					
V_{IH}	Input HIGH Voltage	V_{CC} = Max. (Note 3)	2.0 V		
V_{IL}	Input LOW Voltage	V_{CC} = Max. (Note 3)			0.8 V
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = –18 mA			–1.5 V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V			50 µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.4 V			–400 µA
I_I	Input Leakage Current	V_{CC} = Max., V_{IN} = 5.5 V			50 µA
PECL Outputs: TX,TX; LTX,LTY					
V_{OH}	Output HIGH Voltage	PECL load (Note 4)	V_{CC}–1.025 V		V_{CC}–0.88 V
V_{OL}	Output LOW Voltage	PECL load (Note 4)	V_{CC}–1.81 V		V_{CC}–1.62 V
Power Supplies					
I_{CC1}	V_{CC1} Supply Current	V_{CC1} = V_{CC2} = Max. (Note 5)		15 mA	
I_{CC2}	V_{CC2} Supply Current	V_{CC1} = V_{CC2} = Max.		65 mA	

DC CHARACTERISTICS over operating range unless otherwise specified

Am79866 PDR

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ. (Note 2)	Max.
TTL Inputs: LSCLK, $\overline{\text{LPBCK}}$, TEST					
V_{IH}	Input HIGH Voltage	V_{CC} = Max. (Note 3)	2.0 V		
V_{IL}	Input LOW Voltage	V_{CC} = Max. (Note 3)			0.8 V
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA			−1.5 V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V			50 µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.4 V			−400 µA
I_I	Input Leakage Current	V_{CC} = Max., V_{IN} = 5.5 V			50 µA
TTL Outputs: RDAT 4-0, SDO, RSCLK					
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −1 mA	2.4 V		
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4 mA			0.45 V
I_{SC}	Output Short Circuit Current	V_{CC} = Max., (Note 6)	−15 mA		−85 mA
Differential PECL Inputs: RX,RY; LRX,LRY					
V_{IN}	Input Voltage (Absolute High or Low)	V_{CC} = Max., (Note 3)	2.5 V		V_{CC}
V_{dif}	Input Differential Voltage	V_{CC} = Max., (Note 3,7)	50 mV		1.1 V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC} − 0.88 V			220 µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = V_{CC} −1.81 V	0.5 µA		
Single-ended PECL Input: SDI					
V_{IHS}	Input Single-ended HIGH Voltage	V_{CC} = Max., (Note 3,8)	V_{CC} −1.165 V		V_{CC} −0.88 V
V_{ILS}	Input Single-ended LOW Voltage	V_{CC} = Max., (Note 3,8)	V_{CC} −1.81 V		V_{CC} −1.475 V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC} − 0.88 V			220 µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = V_{CC} −1.81 V	0.5 µA		
Power Supplies					
I_{CC1}	V_{CC1} Supply Current	V_{CC1}= V_{CC2} = Max.		15 mA	
I_{CC2}	V_{CC2} Supply Current	V_{CC1}= V_{CC2} = Max.		120 mA	

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Am79865 PDT

No.	Parameter Symbol	Parameter Description	Test Condition (Note 9)	Min.	Max.	Units
1	t_P	LSCLK Period		40	40	ns
2	t_{PW}	LSCLK Pulse Width HIGH		15		ns
3	t_{PW}	LSCLK Pulse Width LOW		15		ns
4	t_S	TDAT 4-0 to LSCLK Rise Setup Time		12		ns
5	t_H	TDAT 4-0 to LSCLK Rise Hold Time		3		ns
6	t_{R}†	TX,TY,LTX,LTY Rise Time	PECL load	0.3	3	ns
7	t_{F}†	TX,TY,LTX,LTY Fall Time	PECL load	0.3	3	ns
8	t_{SK}†	TX/TY, LTX/LTY Skew	PECL load		±200	ps

Am79866 PDR

21	f_{OS}	LSCLK to received data frequency offset	(Note 10)		±0.25	%
22	t_{PW}	LSCLK Pulse Width HIGH		15		ns
23	t_{PW}	LSCLK Pulse Width LOW		16		ns
24	t_{PW}	RSCLK Pulse Width HIGH	TTL load (Note 11)	10		ns
25	t_{PW}	RSCLK Pulse Width LOW	TTL load (Note 11)	20		ns
26	t_{PD}	RDAT 4-0Valid to RSCLK Rise	TTL load (Note 12)	13		ns
27	t_{PD}	RSCLK Rise to $RDAT_{4-0}$ Invalid	TTL load (Note 12)	10		ns
28	t_S	SDI to LSCLK Rise Setup Time		5		ns
29	t_H	SDI to LSCLK Rise Hold Time		7		ns
30	t_{PD}	LSCLK Rise to SDO Delay	TTL load		30	ns

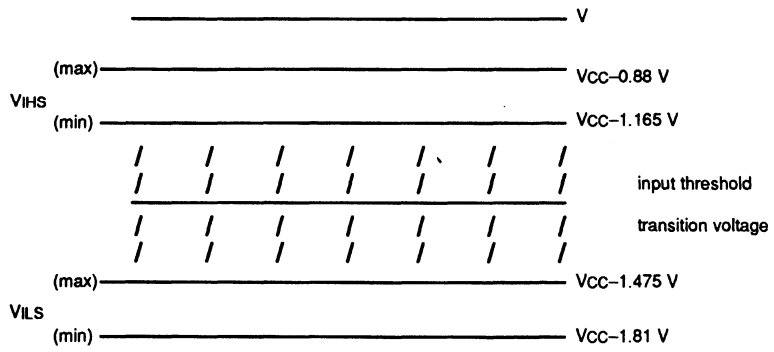
Notes:

†: not included in the production test.

1. For conditions shown as Min. or Max, use the appropriate values specified under operating range.
2. Typical limits are at V_{CC}=5.0 V, 25°C ambient and maximum loading.
3. Typically measured with device in Test mode while monitoring output logic states.
4. Tested for V_{CC}=Min, shown limits are specified over entire V_{CC} operating range.
5. PDT I_{CC1} is tested with all PECL outputs terminated to V_{CC} (unloaded). The PECL outputs contribute 25 mA/pair nominally to I_{CC1} when they are loaded with PECL loads, 50 ohms to (V_{CC}–2). In calculating the chip power dissipation, the contribution by the output loads shall be multiplied by 1 V instead of by V_{CC}.
6. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

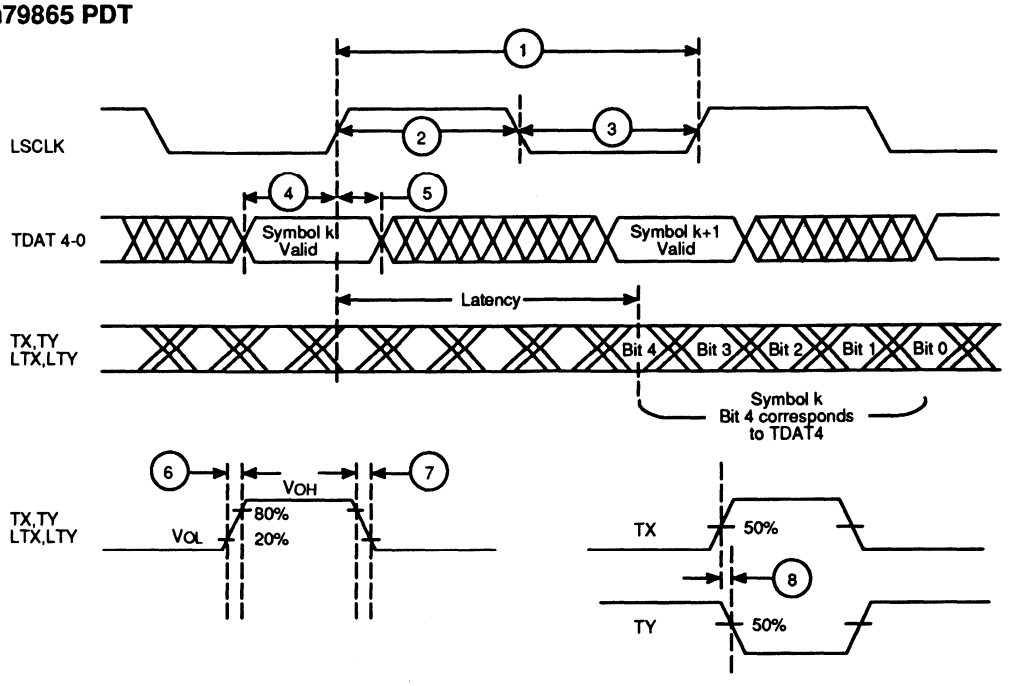
Notes (Continued):

7. V_{dif} is tested with each input voltage within the V_{IN} range.
8. Device thresholds on the SDI pin are verified during production test by ensuring that the input threshold is less than V_{IHS} (min) and greater than V_{ILS} (max). The figure below shows the acceptable range (shaded area) for the transition voltage.



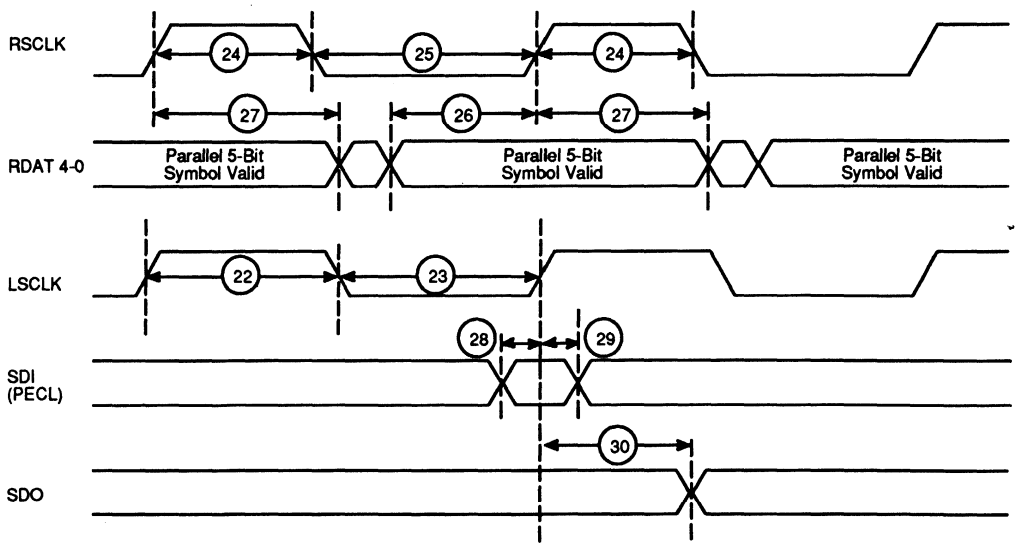
9. All timing references are made with respect to + 1.5 V for TTL-level signals or to the 50% point between V_{OH} and V_{OL} for PECL signals. PECL input rise and fall times must be 2ns±0.2 ns between 20 % and 80 % points. TTL input rise and fall times must be 2 ns between 1 V and 2 V.
10. Received data frequency is determined by serial data inputs. Multiply LSCLK frequency by 5 to convert the receive data bit rate.
11. Tested for 125 MBaud received data rate (1 bit-time is 8 ns). t_{PW}(HIGH) is functionally 2 bit-time wide. t_{PW}(LOW) is functionally 3 bit-time wide.
12. Tested for 125 MBaud received data rate (1 bit-time is 8 ns).

SWITCHING WAVEFORMS
Am79865 PDT



15451-007A

Am79866 PDR



15451-008A

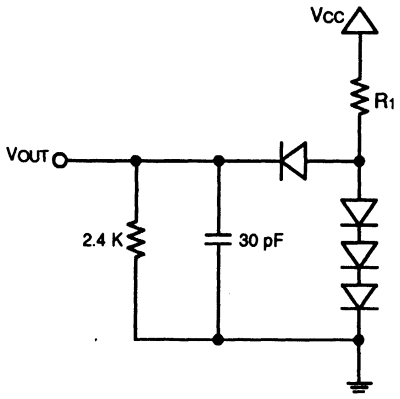
KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

KS000010

SWITCHING TEST CIRCUITS

TTL Output Load

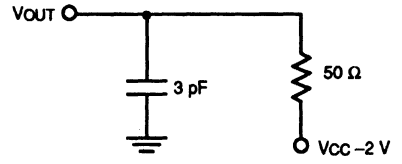


15451-010A

Notes:

1. R_1 = 1 KΩ for the I_{OL} = 4 mA
2. All diodes IN916 or IN3064, or equivalent.
3. C_L = 30 pF includes scope probe, wiring and stray capacitances without device in text fixture.
4. AMD uses constant current (A.T.E.) load configurations and forcing functions. This figure is for reference only.

PECL Output Load



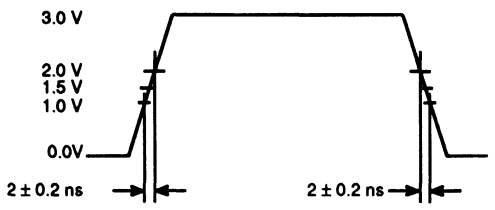
15451-011A

Notes:

1. C_L = 3 pF includes scope probe, wiring and stray capacitances without device in text fixture.
2. AMD uses Automatic test equipment (A.T.E.) load configurations and forcing functions. This figure is for reference only.

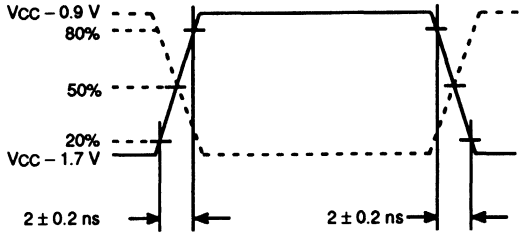
SWITCHING TEST WAVEFORMS

TTL Input Waveform



15451-012A

ECL Input Waveform



15451-013A

FASTcard™ 2

FDDI PC/AT-Based SUPERNET 2 Technology Card (FASTcard)
Dual Attachment Concentrator Board Set and Software Package

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **IBM PC–AT or compatible plug-in board to implement an FDDI station**
- **Highly integrated: single board DAS, 4 master ports per MP board**
- **AMD's FORMAC Plus (Am79C830) and AmPHY (Am79C864, Am79865 and Am79866) second generation FDDI devices**
- **128K byte SRAM buffer memory with parity**
- **Extensive implementation of station management (SMT) services in silicon (including physical connection management (PCM), station insertion and removal, station configuration management and fault detection, isolation and recovery, and duplicate address detection)**
- **Protocol independent—operates with all standard protocols and network operating systems**
- **Built-in interface for external address matching logic (e.g. CAM)**
- **LED status indicators for ring operational and for port A , port B, and master ports physical connection**
- **Station management (SMT) software and device drivers for on-board resources**
- **Complete software support package**
  - pDEMO 2 (demonstration software)
  - FDDINET 2 (device driver and SMT software)
- **Complete documentation**
  - User's manuals for hardware and software
  - SUPERNET 2 Data Book

GENERAL DESCRIPTION

Fiber Distributed Data Interface (FDDI) is quickly becoming the high performance networking protocol for the next generation of local area networks. Its 100 Mbits/s data rate, 100 kilometer network coverage and 500 station connections allow you to increase your productivity and communication between multiple business locations. Currently, FDDI is used as a fiber optic backbone to connect existing Ethernet and Token Ring networks. As applications for engineering workstations become more demanding and data-intensive, the requirement for FDDI's bandwidth becomes necessary as a frontend solution. Advanced Micro Devices is dedicated to providing and enhancing this emerging technology thereby giving you the ability to offer this new standardized technology to accommodate your customer's growing needs.

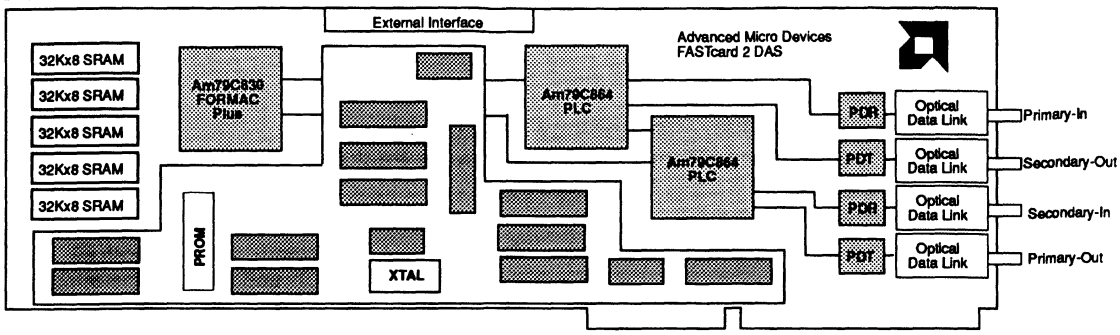
The FASTcard 2 is a PC/AT-based, single MAC, dual attachment FDDI concentrator board-set, based on AMD's second generation SUPERNET 2 FDDI devices. The board set consists of two board types: a dual attachment station (DAS) board, and a master ports (MP) board. The basic 2-board set configures a 4-station dual attachment concentrator. By adding additional MP boards, 8-station or 12-station dual attachment concentrators can be configured.

The FASTcard 2 evaluation board uses AMD's proven SUPERNET 2 hardware solution to operate as an FDDI compliant node. The kit can be used as a model design to base new FDDI development on or it can be used to debug and test your existing system. The hardware and software have been tested and revised to make them more robust and interoperable with multiple vendors' equipment. In fact, you can use the FASTcard 2 tools to check your own system for interoperability.

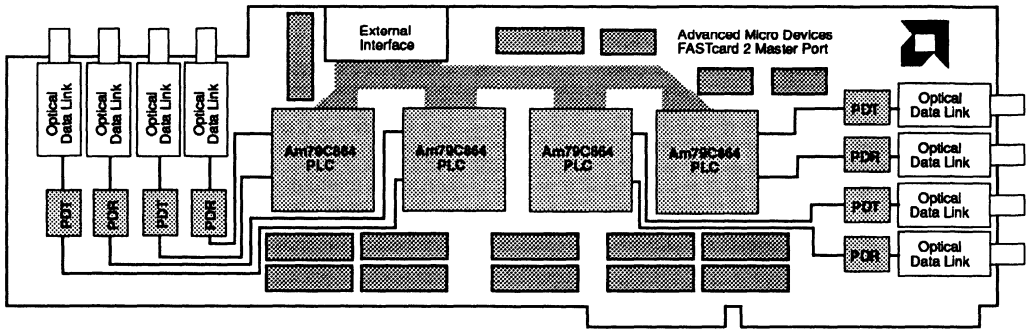
The FASTcard 2 provides complete hardware and software tools to implement a FDDI Dual Attachment Station (DAS) or a concentrator. Along with the board, the DAS card comes with pDEMO 2 (a user interface application), user manuals, SUPERNET 2 databook, ribbon cable and connectors, and 10 foot fiber optic cables and connectors. The Master Port board(s) may be purchased separately to configure a 4, 8 or 12 station dual attachment concentrator.

Advanced Micro Devices offers more than just silicon; we offer the technology, expertise, and support to make FDDI a reality for you. AMD's FASTcard 2 hardware and FDDINET 2 software will reduce your time to market by shortening your development cycle thus allowing you to be at the forefront of the FDDI technology. The tools developed by AMD will also assist you in becoming proficient in this leading edge technology. If the FASTcard 2 and FDDINET 2 kits offer the industry advantage you have been waiting for, contact your local sales representative for more information.

Publication# 16047 Rev. A Amendment/0
Issue Date: September 1991



DAS Card



MP Card

HARDWARE

The FASTcard 2 hardware consists of two main sections; the FDDI station logic and the associated interface logic. The FDDI station logic consists of the SUPERNET 2 chip set, the buffer memory, and the fiber optic transmitter/receiver. The chip set performs the buffer memory management tasks in addition to the MAC and PHY layer functions. The buffer memory on the FASTcard 2 hardware consists of 128k Bytes organized as 32k x 36 bits. Buffer memory control logic provides the host CPU with direct access to the FDDI buffer memory via the host DMA interface of the FORMAC Plus (Am79C830). The chip set also provides interfaces to Station Management (SMT) through the FDDINET 2 software.

The interface logic consists of the AT bus interface, the host-buffer memory interface, counter and interrupt logic, Connection Management (CMT) logic, and FDDI configuration hooks and control logic. The CMT logic is responsible for gathering connection statistics of the network to report them to the station. The DAS board provides interface signals to additional MP cards when constructing a concentrator. The DAS board makes use of the AT's processor as the host and node controller.

SOFTWARE

The FDDINET 2 is a software program that interfaces to LLC, the top sublayer of layer 2 in the OSI model, and runs under the VRTX real-time kernel. It implements three main functions; the chip set drivers, additional MAC services not implemented by hardware, and the up-to-date SMT state machines. It handles MAC functions such as generating frame statistics and handling service requests. The SMT functions implemented by FDDINET 2 include CMT, station statistics, self tests, and overall control of the station. In addition to the required services, FDDINET 2 provides several optional features outlined in the SMT document. FDDINET 2 also supports asynchronous and synchronous frame transmission and ring map generation. The source code is written in "C" and is offered as a separate development tool called the FDDINET 2. AMD provides new revisions to FDDINET 2 as the SMT specification is enhanced and as additional interoperability tests are completed.

pDEMO 2, the application layer interface, provides the ability to control FDDINET 2. With pDEMO 2's interactive menu-driven display, you can select a variety of commands ranging from monitoring frame and counter information to accessing remote parameters from other stations on the network. In addition, pDEMO 2 software and the FASTcard 2 hardware can be used to communicate with FDDI stations, manufactured by other vendors, on a standard FDDI cabled network. pDEMO 2 allows you to experiment with FDDI station operational parameters. While some default values exist to guarantee interoperability, you can input alternate values and observe the results while your station uses the new values. Together, pDEMO 2 and FDDINET 2 give you total control of the FDDI station.

ORDERING INFORMATION

The hardware and software can be ordered using the following ordering part number.

Ordering Part Number (OPN)	Description
AmFDDI-PC-DAS	Dual Attachment Station (DAS) Board
AmFDDI-PC-MP	4-port Master Port (MP) board
AmFDDI-PC-CON	Concentrator board set (1-DAS, 1-MP)
AmFDDI-NET-2	Source code for concentrator board set

For more information, please contact your local AMD sales office.

Physical Dimensions

Am79C830 FORMAC Plus

CGX169
169-Lead Pin Grid Array without Heat Sink 6–2

PQJ 168
168-Pin Plastic Quad Flat Pack (Trimmed and Formed) 6–3

PQR168
168-Pin Plastic Quad Flat Pack (TapePak) 6–4

Am79C864 Physical Layer Controller

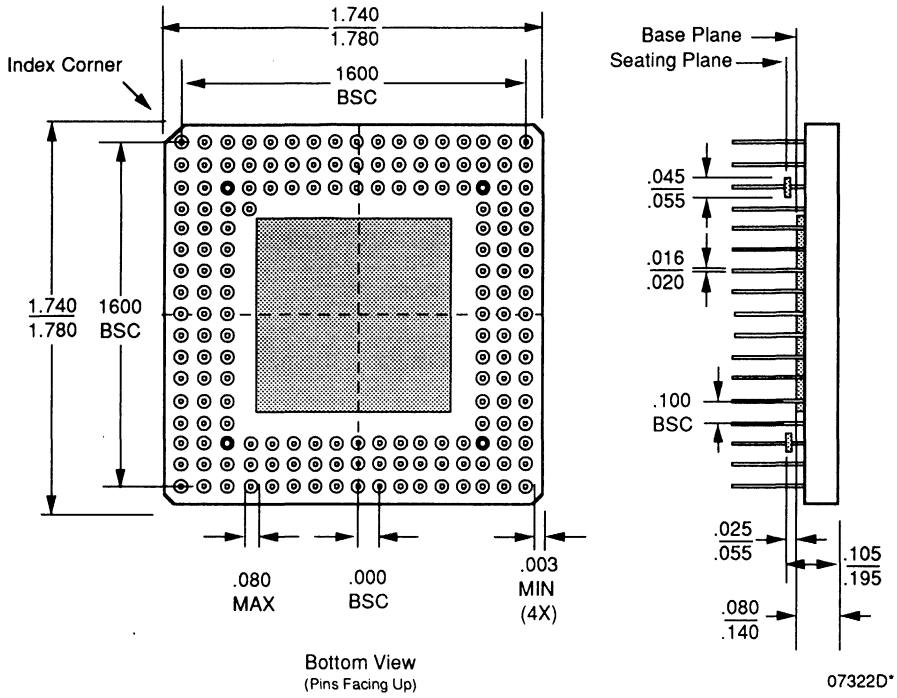
PQJ120
120-Pin Plastic Quad Flat Pack (Trimmed and Formed) 6–5

PQR120
120-Pin Plastic Quad Flat Pack (TapePak) 6–6

Am79865/Am79866 Physical Data Transmitter/Physical Data Receiver

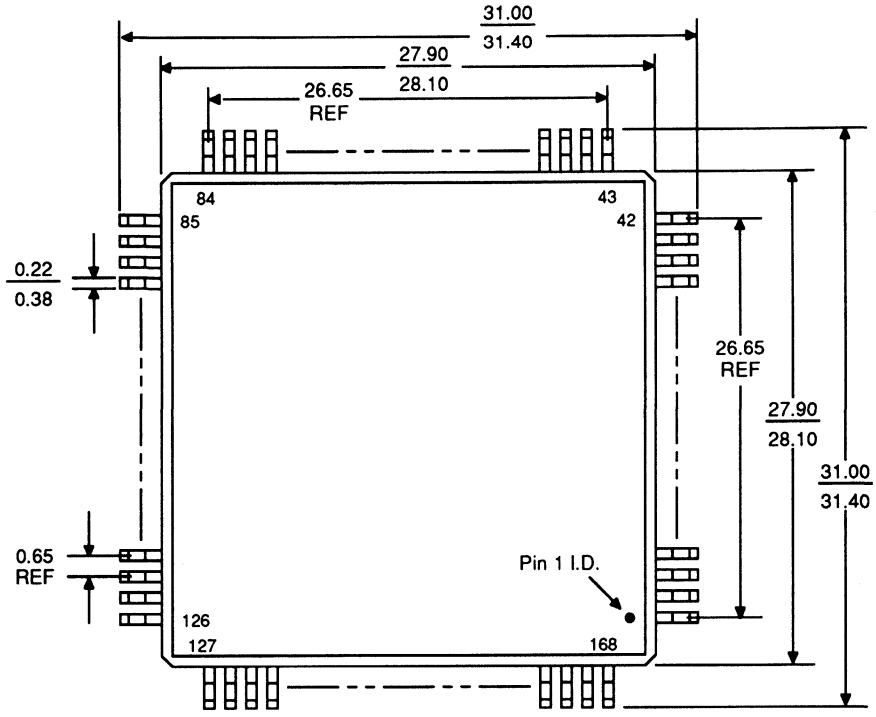
PL 020
20-Pin Plastic Leaded Chip Carrier 6–7

Am79C830 FORMAC Plus
CGX169
169-Lead Pin Grid Array without Heat Sink

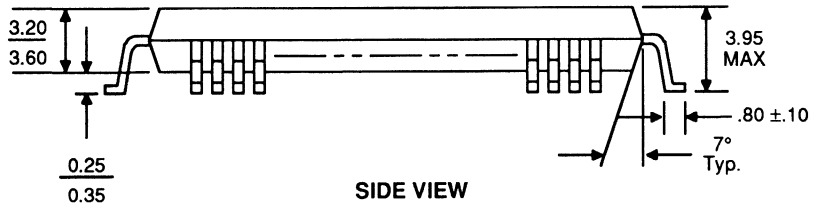


For reference only. All dimensions are measured in inches unless otherwise noted. BSC is an ANSI standard for Basic Space Centering.

Am79C830 FORMAC Plus
PQJ168
168-Pin Plastic Quad FlatPack (Trimmed and Formed)



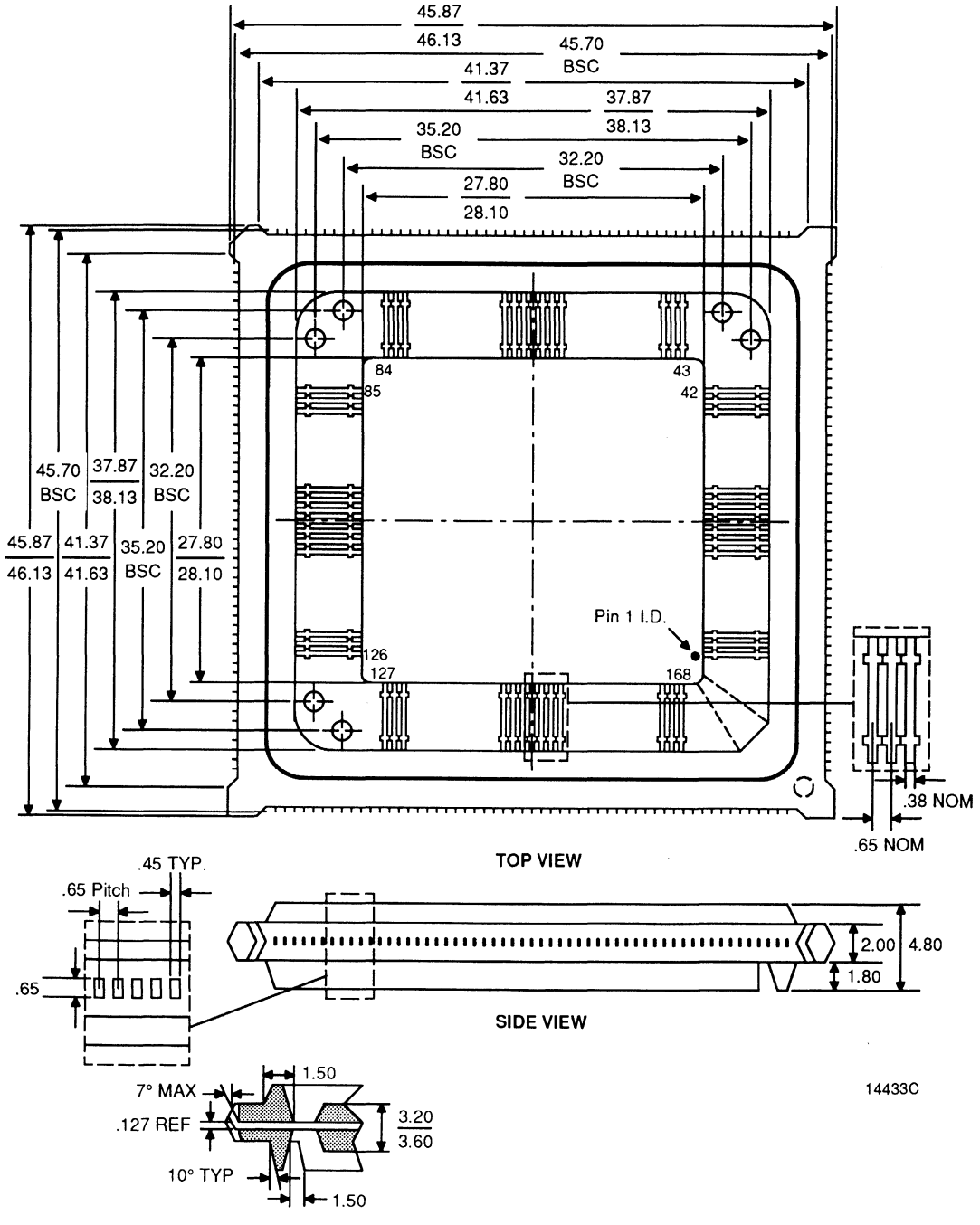
TOP VIEW



SIDE VIEW

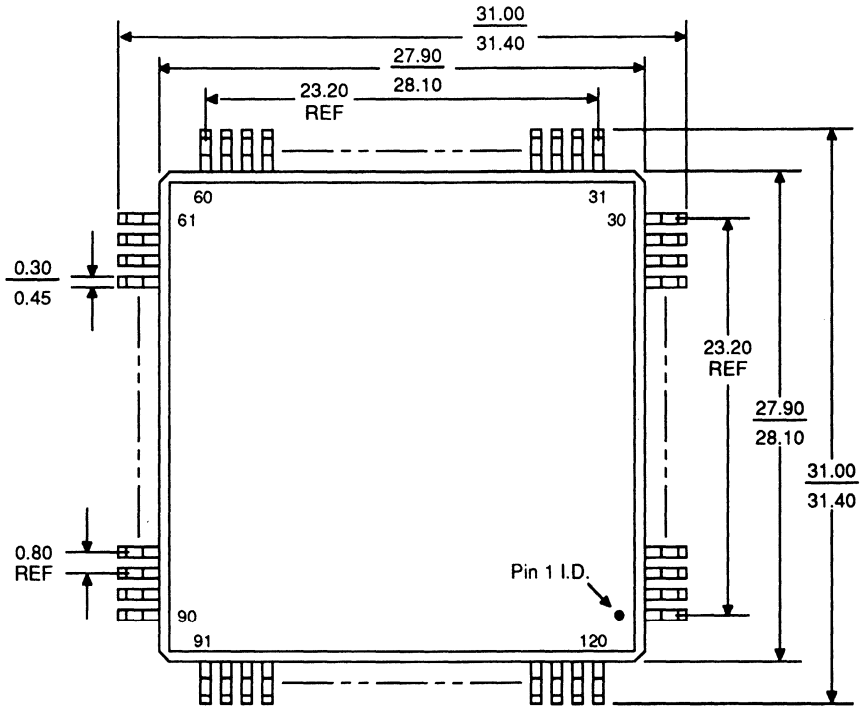
For reference only. All dimensions are measured in millimeters. BSC is an ANSI standard for Basic Space Centering.

Am79C830 FORMAC Plus
PQR168
168-Pin Plastic Quad FlatPack (TapePak)

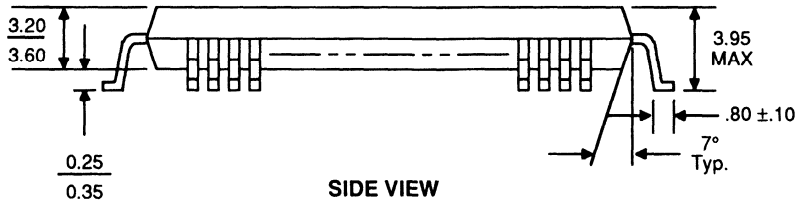


For reference only. All dimensions are measured in millimeters. BSC is an ANSI standard for Basic Space Centering.

Am79C864 Physical Layer Controller
PQJ120
120-Pin Plastic Quad FlatPack (Trimmed and Formed)



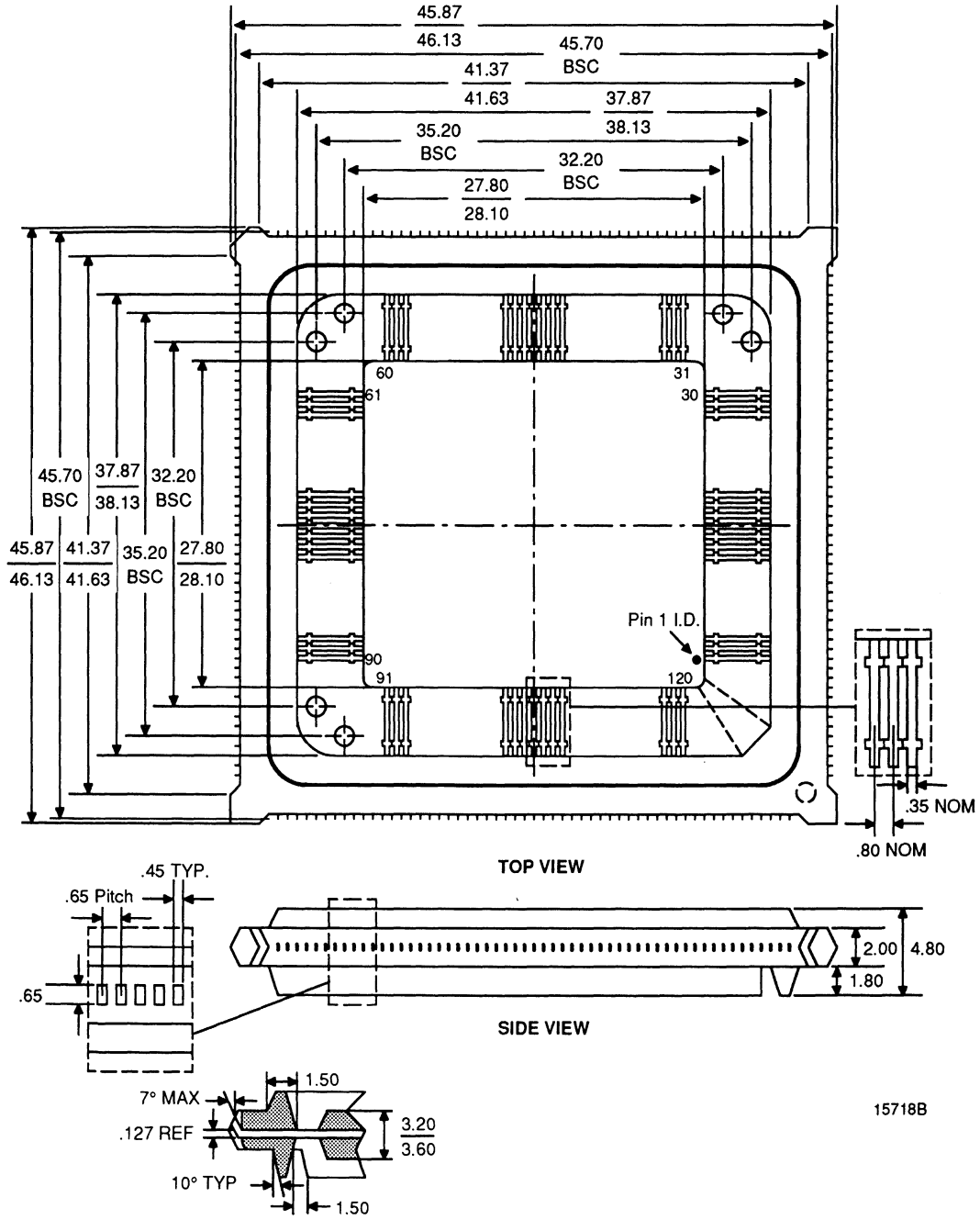
TOP VIEW



SIDE VIEW

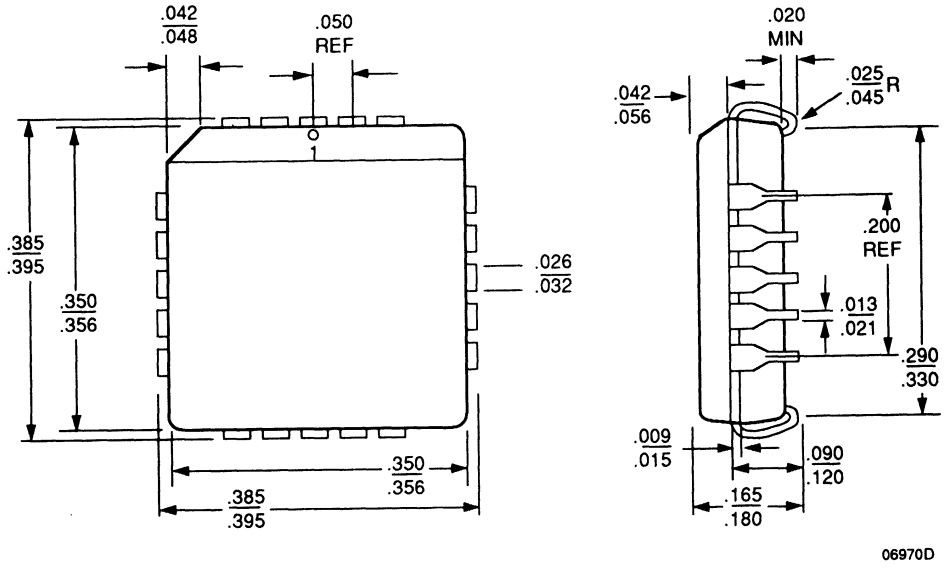
For reference only. All dimensions are measured in millimeters. BSC is an ANSI standard for Basic Space Centering.

Am79C864 Physical Layer Controller
PQR120
120-Pin Plastic Quad FlatPack (TapePak)



For reference only. All dimensions are measured in millimeters. BSC is an ANSI standard for Basic Space Centering.

Am79865/Am79866 Physical Data Transmitter/Data Receiver
PL 020
20-Pin Plastic Leaded Chip Carrier



For reference only. All dimensions are measured in inches unless otherwise noted. BSC is an ANSI standard for Basic Space Centering.

APPENDIX A

INTERFACE CONNECTION DIAGRAMS

Interfacing connection of the FORMAC Plus (Am79C830) with the Physical Layer Controller (Am79C864).

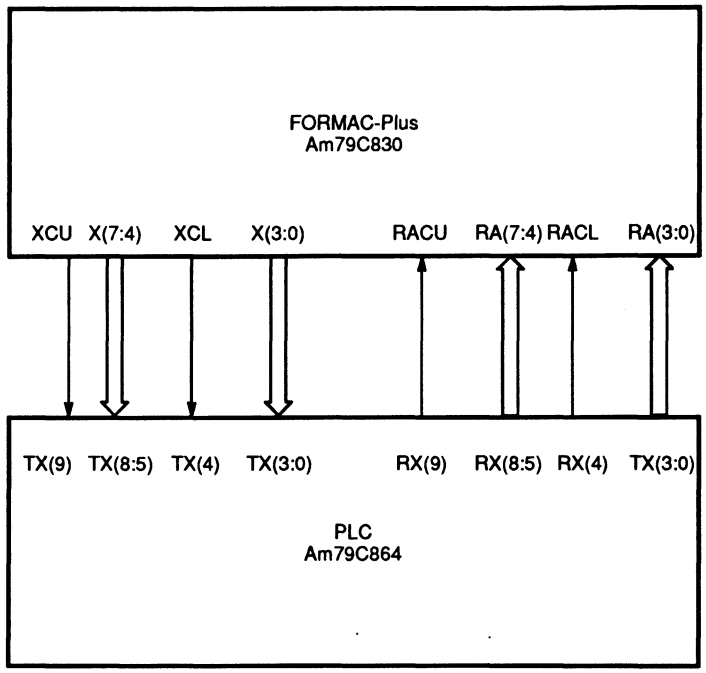


Figure A-1. Interface Connection Diagram Between FORMAC Plus and a PLC for Single Attachment Station (SAS).

Note:

The above diagram is for a Single Attachment Station (SAS). RB-Bus (of FORMAC Plus) can be used instead of RA-Bus. The TXPAR line should be grounded and the RXPAR line left unconnected since FORMAC Plus does not generate a parity bit for X-Bus. Therefore, the software must mask out the interrupt generated from PLC due to parity error.

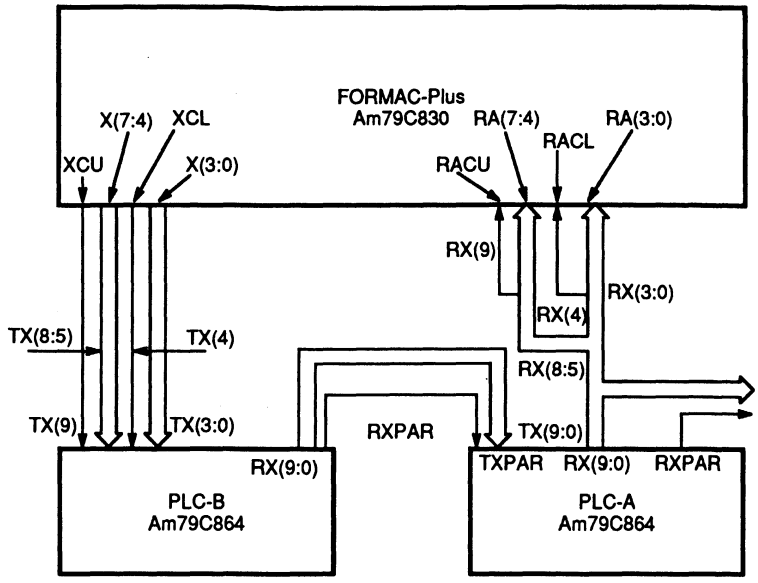


Figure A-2. Interface Connection Diagram Between FORMAC Plus and Two PLCs for Single MAC Dual Attachment Station (SMDAS) Without an External MUX.

Note:

The above shows the connections between a FORMAC Plus and two PLCs (i.e., for a Single MAC Dual Attachment Station) without any external MUX. THRU_B configuration cannot be realized with this connection. TXPAR of PLC-B is grounded. RA-Bus and RB-Bus could be interchanged.

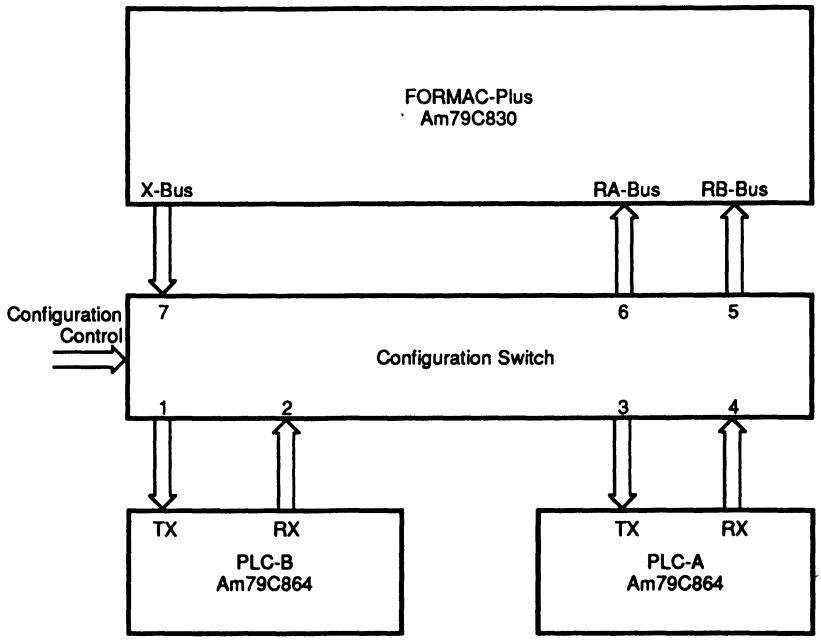


Figure A-3. Interface Connection Diagram Between FORMAC Plus and Two PLCs for Single MAC Dual Attachment Station (SMDAS) With an External MUX.

Note:

The above shows the connection between a FORMAC Plus and two PLCs for a Single MAC Dual Attachment (SMDAS) station. This connection will support THRU_B configuration. The Configuration Switch contains 7 paths (3 input and 4 output). The following table shows the connection between different paths for different "Configuration Control".

Configuration Control	Connection Paths
Isolated	2-1, 4-3
Wrap_A	4-5, 7-3, 1-2
Wrap_B	2-5, 7-1, 3-4
Thru_A	4-5, 7-1, 2-3
Thru_B	2-5, 7-3, 4-1

Interfacing Connection of the Physical Data Transmitter (Am79865 PDT)/Physical Data Receiver (Am79866 PDR) with the Physical Layer Controller (Am79C864 PLC) and the Physical Medium Dependent (PMD) Optical Transceiver.